# A 2.4 GHz Multi-Channel FBAR-based Transmitter With an Integrated Pulse-Shaping Power Amplifier

Arun Paidimarri, *Student Member, IEEE*, Phillip M. Nadeau, *Student Member, IEEE*, Patrick P. Mercier, *Member, IEEE*, and Anantha P. Chandrakasan, *Fellow, IEEE*

***Abstract*—A 2.4 GHz TX in 65 nm CMOS defines three channels using three high-Q FBARs and supports OOK, BPSK and MSK. The oscillators have −132 dBc/Hz phase noise at 1 MHz offset, and are multiplexed to an efficient resonant buffer. Optimized for low output power ≈ −10 dBm, a fully-integrated PA implements 7.5 dB dynamic output power range using a dynamic impedance transformation network, and is used for amplitude pulse-shaping. Peak PA efficiency is 44.4% and peak TX efficiency is 33%. The entire TX consumes 440 pJ/bit at 1 Mb/s.**

***Index Terms*—BAN, body area networks, BPSK, FBAR, MEMS, MSK, multi-channel, OOK, pulse shaping, resonant buffer, RF resonator, transmitter, TX, -10 dBm, 24 GHz.**

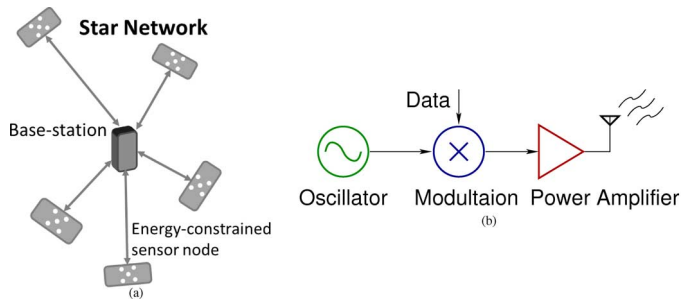



Fig. 1. (a) Star topology, a common network architecture for Body Area Networks. (b) The main blocks of a generic transmitter.

## I. Introduction

BODY Area Networks (BANs) for continuous health monitoring and sports fitness applications are becoming increasingly common in day-to-day life and are being enabled by improvements in sensor and circuit technologies. Wireless connectivity is an integral part of such systems, and generally accounts for a large portion of the system power consumption [1]. With an increasing push towards energy-harvested and/or battery-less operation, the energy constraints on the system are becoming tighter, and there is a need to explore the most efficient wireless transmit solutions. An ultra-low power transmitter architecture for such a system is developed in this work.

BANs typically operate in a star-topology [2], shown in Fig. 1(a). The energy-constrained sensor communicates with a relatively energy abundant base-station like a cell-phone, which then further transmits the data to health-care providers over well-established long-distance networks. The range of communication needs to be about 2 m. The path loss in a typical around-the-human-body link is about 60–70 dB, approaching 80 dB in the worst case [3]. The receive sensitivity of a typical 2.4 GHz ISM-band radio, like Bluetooth, is at least −90 dBm [4], which implies that a nominal transmit power of −10 dBm on the sensor node is sufficient for reliable communication. This output power level is also the recommended transmit power in the IEEE802.15.6 BAN standard [2].

Hence, the transmitter architecture must be optimized considering these low radiated output power levels. A generic transmitter architecture is shown in Fig. 1(b). It requires a Local Oscillator (LO), modulation blocks, and a power amplifier. For a −10 dBm, or 100 $\mu$W output power, the PA is no longer the dominant power consumer, and the power of the remaining blocks starts to dominate. If simple binary modulation schemes are used, the power of modulation can be greatly reduced, as is done in [5], [6]. This reduces the problem to developing efficient LO generation schemes. In this work, OOK, BPSK and MSK are implemented.

Multiple schemes have been employed in the literature to generate efficient LOs for low power transmitters. The PLL in [7], for example, is duty-cycled and turned on only just before the packet transmission occurs. This reduces the peak power consumption of the transmitter. The PLL allows the LO to be set at any frequency, however, this comes with a slow startup time due to the finite bandwidth of the PLL. A slow frequency-correction-loop is employed in [5], [8]. The base-station, which has an accurate frequency sends correction signals to the sensor node. The energy-penalty on the sensor node is negligible. However, for very low duty-cycle applications, this scheme is difficult to implement, since the drift in the sensor node frequency can become large.

Another approach is to use high-Q direct-RF resonators that provide stable oscillation frequencies at RF, eliminating the need for a PLL. Film Bulk Acoustic wave Resonators (FBAR) or Surface Acoustic Wave (SAW) resonators have been used as frequency references in [6], [9], [10]. The circuit model of these resonators is shown in Fig. 2, along with the impedance plot of a representative FBAR. The device has a series resonance where it presents a low impedance and an intrinsic parallel

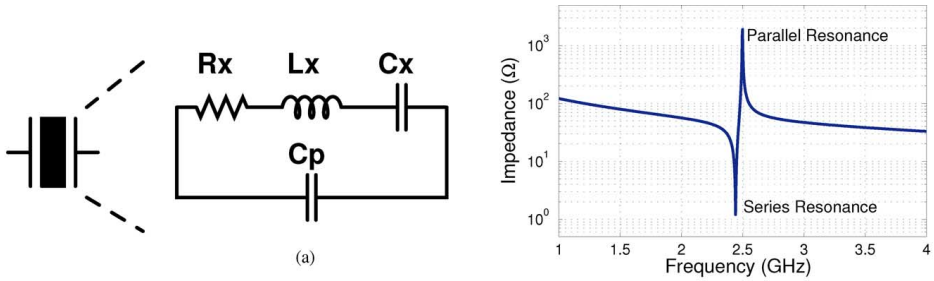
Manuscript received August 31, 2012; revised November 21, 2012; accepted December 12, 2012. Date of publication January 30, 2013; date of current version March 22, 2013. This paper was approved by Guest Editor Vivek De. This work was supported by the Interconnect Focus Center, one of six research centers funded under the FCRP, an SRC entity.

A. Paidimarri, P. M. Nadeau, and A. P. Chandrakasan are with the Massachusetts Institute of Technology (MIT), Cambridge, MA 02139 USA (e-mail: arun_p@mit.edu; anantha@mtl.mit.edu).

P. P. Mercier is with the University of California at San Diego, La Jolla, CA 92093 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2013.2239001




| $R_x(\Omega)$ | $L_x$(nH) | $C_x$(fF) | $C_p$(pF) | $Q$ | $R_p(\Omega)$ |
|---|---|---|---|---|---|
| 1.05 | 107.2 | 38.99 | 1.292 | 1600 | 2.26 |

(c)

Fig. 2. Circuit model for RF resonators and the impedance profile of a representative FBAR. (a) Butterworth Van Dyke model for resonators. (b) Impedance characteristics of a representative FBAR. (c) Sample model values for FBARs used in this work.

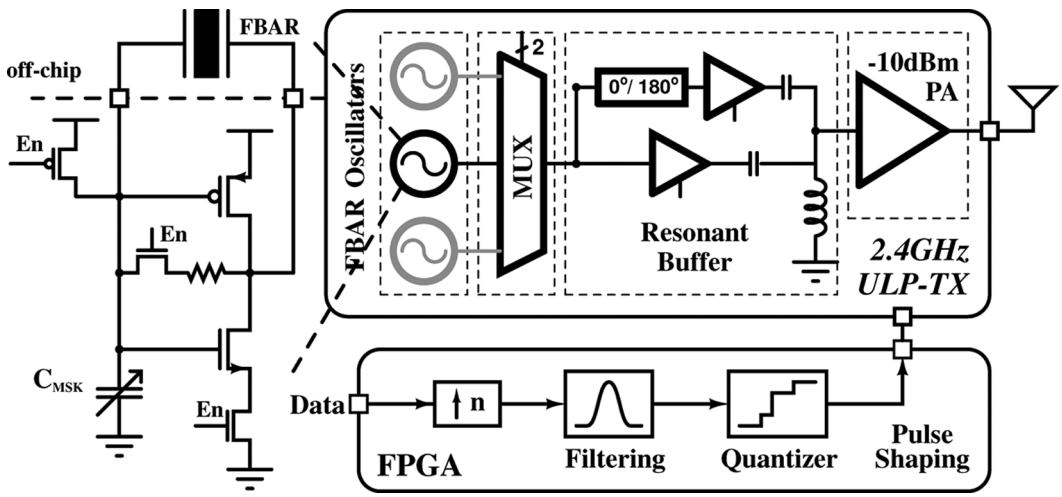



Fig. 3. TX architecture with the FBAR oscillator of one channel.

resonance where it has a high impedance. Most oscillators use this parallel resonance [11], where the high impedance results in higher gain, allowing for low current consumption in the oscillator.

The parallel resonance frequency can be shifted lower by capacitive loading, but this also brings down the parallel resonance impedance, thus increasing power consumption and reducing the filtering provided by the resonator. Typically, the frequency tuning of these oscillators is limited, and one resonator operates only in one frequency channel [9]. However, in an increasingly congested band such as the 2.4 GHz ISM band, multi-channel operation is essential for reliable communication. This can be achieved by adding resonators with different parallel resonance frequencies to define channels, and having an architecture that can efficiently select/multiplex between them. Such two-channel implementations have been demonstrated in [6], [9], but these architectures are not as scalable to a large number of channels.

This work aims to exploit the advantages of low power, frequency stability and low noise provided by the resonators, and address the issue of single-channel operation by developing a scalable multi-resonator multi-channel architecture. FBARs are used to demonstrate the ideas in a three-channel implementation. Also, the architecture is optimized to provide high transmit efficiencies for the low $-10$ dBm output power levels typical in BANs.

## II. Transmitter Architecture

The multi-channel FBAR-based transmitter architecture is shown in Fig. 3 [12]. Multi-channel capability is achieved through the use of multiple oscillators, each attached to one FBAR. The outputs of the oscillators are then multiplexed through transmission gates onto a low input capacitance resonant buffer. This buffer then drives an efficient push-pull type power amplifier. The architecture supports three modulation schemes, OOK, BPSK and MSK at data rates up to 1 Mbps, all with pulse-shaping capability for improved spectral efficiency. Phase inversion for the BPSK modulation is achieved through an alternate path in the buffer stage that employs matched but inverted delays.

For the pulse shaping, rather than employing a linear mixer and linear power amplifier, the architecture employs a polar scheme. Amplitude modulation is achieved through a digitally tuned impedance transformation network that is part of the PA.

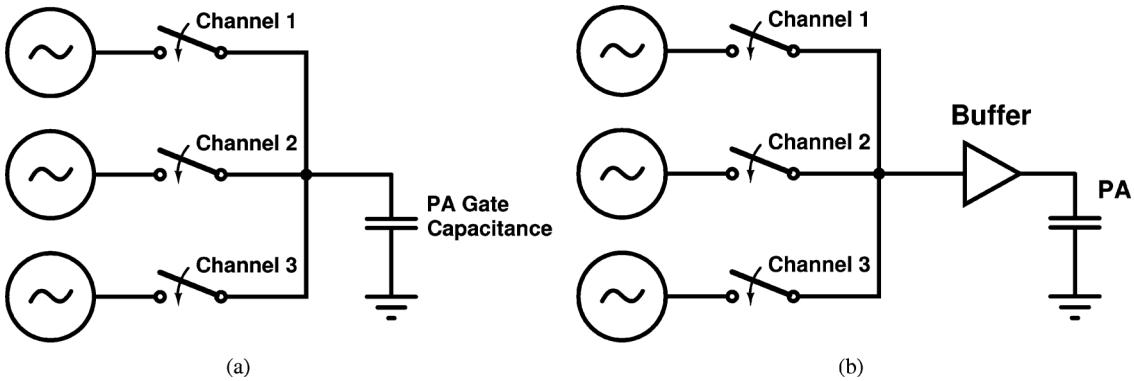



Fig. 4. Two multiplexing schemes. (a) Direct multiplexing of oscillators to PA. (b) Multiplexing of oscillators to PA with a buffer.

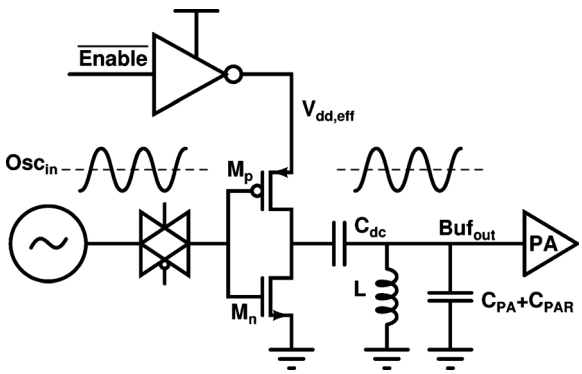



Fig. 5. Resonant buffer used in multiplexing oscillators to the PA.

The digital logic implementing the pulse shaping based on the input data is implemented in an FPGA. The input data is up-sampled at a chosen oversampling speed (typically between 8× to 10× the data rate) and then passed through the appropriate filter (Gaussian for OOK and MSK, and Square Root Raised Cosine for BPSK). The outputs are then quantized to the levels that can be generated by the chip, and the corresponding digital signals are sent to the chip.

A low voltage design (0.7 V) coupled with rail-to-rail swing on all RF nodes is used for improved power efficiency of the transmitter. Full swing on the oscillator minimizes short-circuit current in the buffers, while full swing at the input of the PA maximizes overdrive. Each of the individual circuit blocks in the architecture are explained in detail in the following sections followed by the measurement results.

## III. FBAR Oscillators

Resonator-based oscillator designs, including with FBARS, have been studied extensively in the literature [11], [13], [14]. The high-Q and frequency stability of the resonator, consequences of their mechanical properties, enables stable LO generation. The high-Q also results in low phase noise, and the intrinsic stability of the resonator allows for PLL-less systems, achieving fast startup times.

An inverter-style Pierce oscillator topology is chosen in this work [13]. The schematic is shown in Fig. 3. This topology was chosen because it provides rail-to-rail output, which is important for driving the next stage efficiently. Also, due to the current re-use in the NMOS and PMOS, the power consumption is reduced by 2× compared to an NMOS-only implementation. The inverter is biased at mid-rail through the bias resistor. The current of the circuit at this bias point should be such that the startup condition, $g_{\rm m} > g_{\rm m,crit}$ is met, where $g_{\rm m,crit}$ is the critical transconductance below which oscillations cannot be sustained [14]. The oscillator has an *enable* signal to turn on/off the particular channel.

The oscillator is operated at a lower-than-nominal voltage in order to reduce undesired short-circuit power in the NMOS and PMOS devices. As the supply voltage lowers, the devices become biased in the sub-threshold region, which further improve their transconductance efficiency. However, biasing the devices too deep into subthreshold requires a proportional increase in their size to achieve start-up, thereby significantly increasing parasitic capacitance, which loads the FBAR and brings down the effective parallel resonance impedance. Taking these issues into consideration, this work employs a 0.7 V power supply for the oscillator.

### A. MSK Modulation

One way of implementing Minimum Shift Keying (MSK) is through FSK modulation by setting the deviation to be $0.25 \cdot DataRate$. Hence, in order to achieve MSK modulation at 1 Mbps, center frequency tuning of ±250 kHz must be provided. This is achieved by a digitally controlled capacitor bank $C_{\rm MSK}$ of 150 fF, as shown in Fig. 3. This number has been calculated, through simulations, for the worst-case resonators, which corresponds to the highest resonator-Q. Since the digitally switched capacitors have a finite $Q_{cap}$, they present an effective resistive load on the oscillator, given by $R_{\rm eff} = Q_{cap} \cdot 1/\omega C_{Load}$. This effective resistive load (about 5–10 kΩ) is designed to be much larger than the intrinsic parallel resonance impedance of the FBAR (about 2 kΩ for the resonators used in this work).

### B. Considerations for Multi-Channel Capability

Since direct multiplexing of the high-Q FBARs is not feasible, multi-channel capability is achieved by replicating the

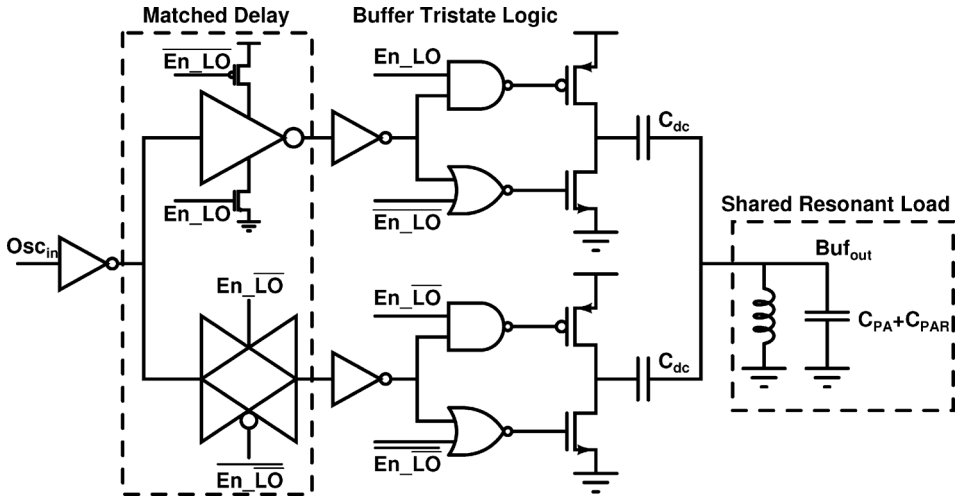



Fig. 6. Resonant Buffer with capability to generate $LO$ and $\overline{LO}$ for BPSK modulation.

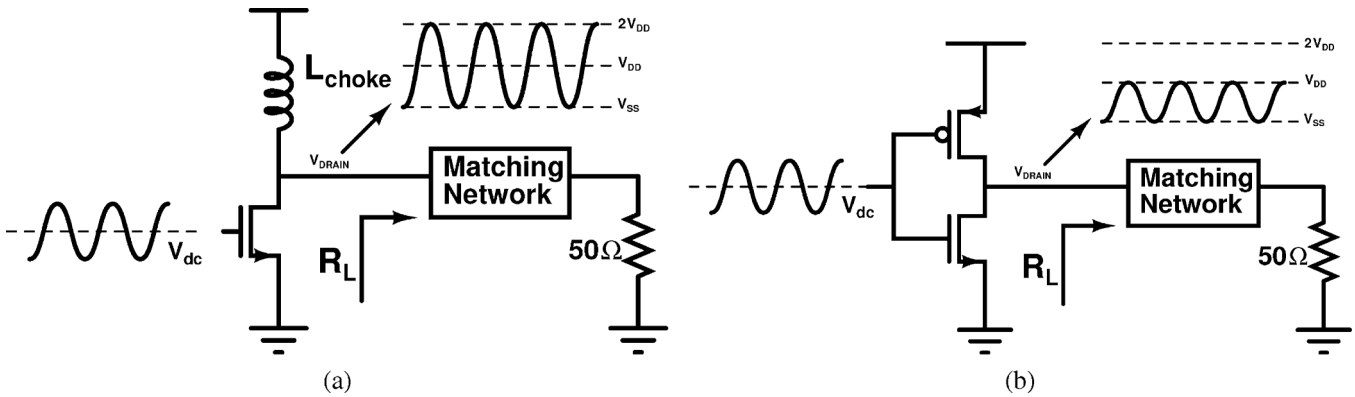



Fig. 7. Two canonical PA topologies considered.(a) NMOS-only PA topology. (b) Inverter-based push-pull PA topology.

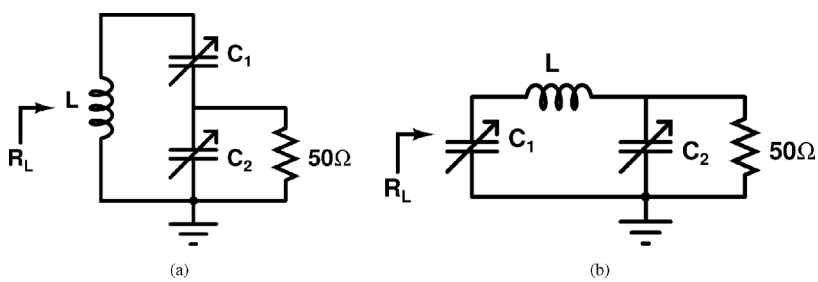



Fig. 8. Tapped capacitor and $\pi$ matching networks. (a) Tapped capacitor match. (b) $\pi$-match.

oscillator circuits for each resonator. However, since each resonator is about 400 $\mu$m $\times$ 600 $\mu$m, the floor-planning of the chip becomes important. It is essential that the bondwires used to connect the resonator to the chip be as short as possible. This is because the bondwire inductance can cause parasitic oscillations with the parallel capacitance $C_P$ of the FBAR and the parasitic capacitors of the oscillator [15]. The shorter the bondwires, the higher the parasitic oscillation frequency, and the less likely it is to affect the circuit, since, the bondwire resistance also increases with frequency. Simulations suggest that the bondwires be under 400 $\mu$m, in which case, the parasitic oscillations would have to occur at frequencies greater than 15 GHz. The floor-planning problem is solved by connecting the three resonators to three different sides of the chip, as shown in the package photo in Fig. 12(b).

## IV. FBAR Oscillator Multiplexing for Channel Selection

Since one FBAR oscillator defines a single channel, multi-channel operation in this architecture is achieved through oscillator multiplexing. The input to this block is a rail-to-rail swinging signal generated by the Pierce oscillator. The output must be a rail-to-rail swinging signal driving the PA, which presents about 200 fF input capacitance. Two methods for multiplexing are considered.

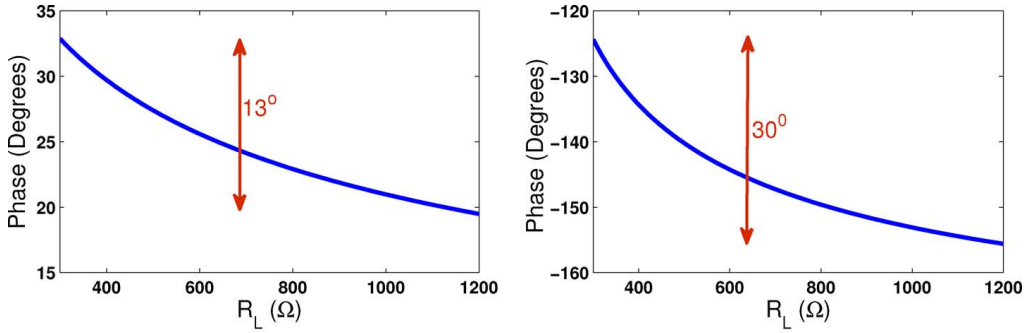



Fig. 9. Variation of phase of output with changing impedance settings for tapped capacitor match and $\pi$-match. (a) Tapped capacitor match. (b) $\pi$-match.

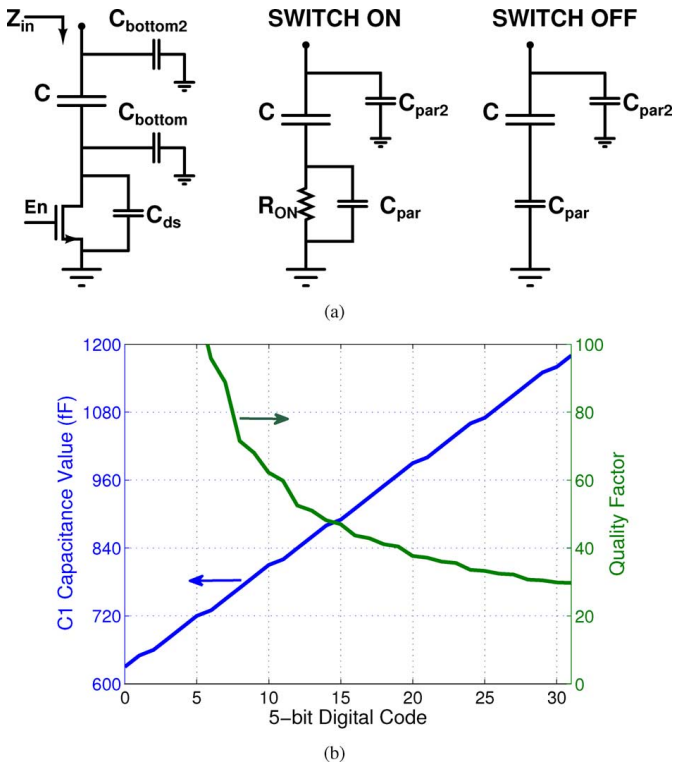



Fig. 10. (a) Design of capacitor banks in the PA. (b) Simulated characteristics of bank $C_1$.

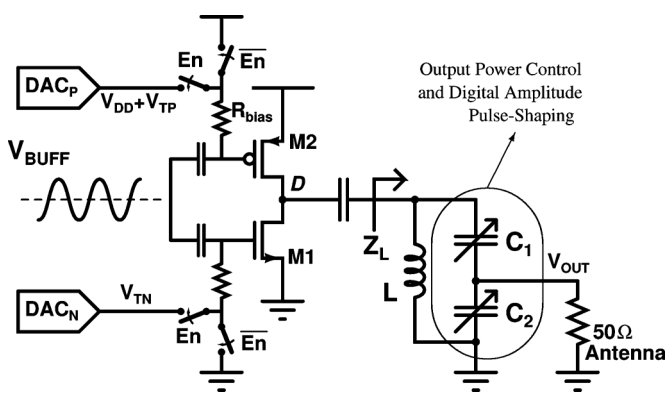



Fig. 11. Integrated PA with pulse-shaping using dynamic impedance transformation.

### A. Direct Multiplexing to the PA

Shown in Fig. 4(a), this scheme ideally has near zero power overhead, since the PA capacitance is in resonance with the oscillator. The effective Q of this capacitance presents an equivalent resistive load to the oscillator, which de-Qs it, increasing power consumption.

The following analysis calculates the effective resistance seen by the oscillator. Let $C_L$ be the capacitance of the load that is being multiplexed. Let $C_P$ be the parasitic capacitance of each transmission gate as seen on the load side. Thus, if the number of channels multiplexed is $n$, the total capacitance presented to the oscillator would be $C_L + nC_P$. Let $R$ be the series resistance of an 'on' transmission gate and note that the product $k = RC_P$ is approximately a constant for a given process. The $Q$ of this load to the oscillator is $1/\omega R(C_L + nC_P)$. The effective loading resistance presented to the oscillator is thus (assuming high-Q):

$$R_P \approx R \cdot Q^2 = \frac{1}{\omega^2 R(C_L + nC_P)^2} \tag{1}$$

$$= \frac{C_P}{\omega^2 k(C_L + nC_P)^2}. \tag{2}$$

For a given $C_L$ and channel number $n$, the maximum $R_P$ is obtained when $C_P = C_L/n$. Thus, the maximum resistance presented to the oscillator is given by:

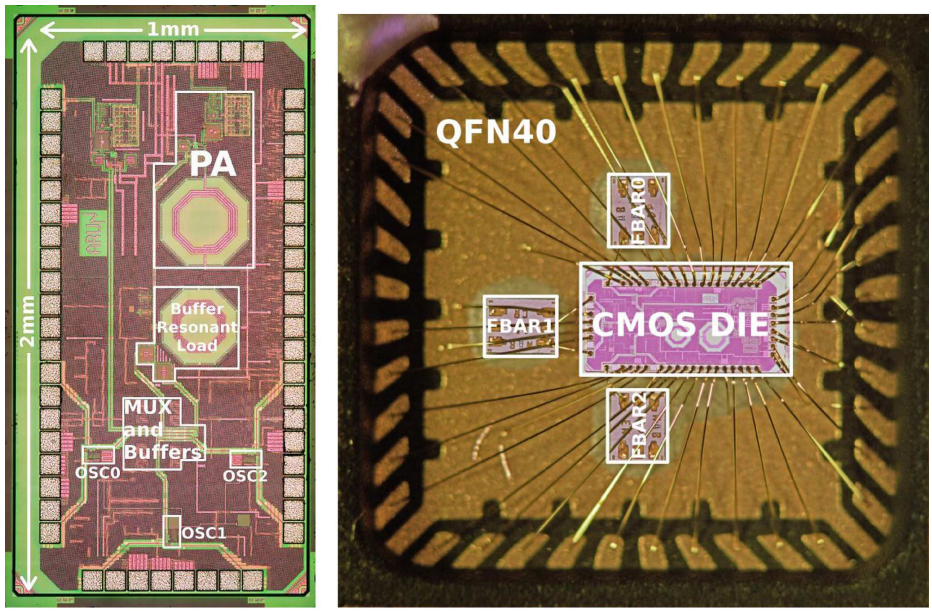
$$R_{P,\max} = \frac{\frac{C_L}{n}}{\omega^2 k(2C_L)^2} = \frac{1}{n} \cdot \frac{1}{4\omega^2 k C_L}. \tag{3}$$

Thus, given a specification for a minimum $Rp$ that avoids oscillator performance degradation, the maximum number of channels possible is given by:

$$n_{\max} = \left\lfloor \frac{1}{4\omega^2 k} \cdot \frac{1}{R_P C_L} \right\rfloor. \tag{4}$$

While multiplexing to the $C_L = 200$ fF PA, if an effective loading of $R_P > 5$ k$\Omega$ is desired, only 1 channel is supported in the 65 nm technology used in this work. For three channel operation, the $R_{P,max} = 2.9$ k$\Omega$ only. Thus, self-loading of the switches limits scaling to a large number of channels.

In addition, the input capacitance to the PA is not a constant. It can vary through the Miller multiplication of the gate-drain capacitance, $C_{gd}$, of the transistors in the PA (see Section V).




(a) (b)

Fig. 12. Die photo of TX and the packaged chip with 3 FBARs. (a) Die photo. (b) Packaging photo.

If this capacitance is connected to the oscillator directly, it will modulate the center frequency.

### B. Multiplexing With A Buffer

The above issues are solved by a different approach, shown in Fig. 4(b). A buffer decouples the problem of multiplexing and large PA input capacitance. The buffer drives the large capacitance, while presenting a much reduced load to the multiplexing circuit, making it much easier to size the transmission gates and scale to a large number of channels.

However, if a simple inverter buffer chain is used, the switching power consumption, $C_{\mathrm{PA}} V_{DD}^2 f_c$ is 250 $\mu$W. This is prohibitive from an efficiency standpoint, considering that the target output power of the PA is 100 $\mu$W. In addition, the power consumption is sensitive to layout parasitics.

### C. Resonant Buffer

This buffer power consumption problem is solved through the use of a resonant buffer topology, shown in Fig. 5. The load capacitance is resonated with an on-chip inductor, similar to techniques used in resonant clock distribution networks [16]. The inverter only needs to provide for the losses in the tank. Since it is driven by rail-to-rail swinging output of the oscillator, no special biasing is required for the circuit. The power consumption of the resonant buffer is:

$$P_{\mathrm{Buf}} = V_{DD} I_{\text{short-circuit}} + \frac{V_{DD}^2}{8 R_{\mathrm{p,ind}}}. \tag{5}$$

The equivalent resistive load $R_{\mathrm{p,ind}}$ is only a very weak function of the capacitance. The larger the value of the capacitance to be resonated, the smaller is the value of the inductor used, which limits the value of the effective load resistance, since $R_{\mathrm{p,ind}} \approx \omega L Q_{\mathrm{ind}}$. Hence, the inductor with the largest possible impedance, after allowing for process variation of the inductor and layout parasitics is chosen. In the process used, the value obtained was about 1 k$\Omega$.

Since the inverter only needs to drive the effective load resistance, and not the total capacitance, the size of the inverter can be very small. A sizing ratio of $<$ 1:10 was achieved, with the input capacitance of the buffer being just 20 fF. With this, the maximum number of channels increases to $n_{\max} = 17$ for $R_P > 5$ k$\Omega$.

The buffer is tristated with the $\overline{enable}$ signal. Since the resonant network is low-Q, and limited by on-chip inductors, the buffer turns on/off within a few RF cycles. The buffer circuit consumes $\approx$ 100 $\mu$W from the 0.7 V supply, a 2.5$\times$ improvement over the inverter buffer chain.

### D. Alternate Buffer Paths for BPSK Capability

Additional parallel paths in the buffer are designed to enable BPSK modulation. Matched but phase-inverted delays are used to generate BPSK modulation in an energy efficient, and digital fashion [17], [18]. The implementation is shown in Fig. 6. The delay of an inverter is nominally matched with the delay of the transmission gate. The final resonant inverter stages in this circuit share the resonant load with the buffer stage described previously in Fig. 5. The signals $en\_LO$ and $en\_\overline{LO}$, which are independent of the $\overline{enable}$ signal of Fig. 5, enable/disable the two paths separately. With this circuit, the input capacitance presented to the multiplexer is only 1 to 2 fF, and hence this scheme can extend to an even larger number of channels than the 17 for the buffer of the previous section. In this case, the performance will be limited by routing capacitance, which is not taken into account in the analysis of (4).

Tristating logic is used as opposed to the power supply cut-off method in order to improve speed, since the enable signals for the buffers switch at the data rate and need to settle in $\ll 100$ ns. This leads to slightly higher power consumption because the

20 fF inverter is driven by logic and is not resonant with the oscillator tank. The overhead is about 30 $\mu$W.

A Monte-Carlo process variation simulation is performed to calculate the phase mismatch variations between the two paths. A standard deviation of 2° is observed. This accuracy is sufficient for BPSK modulation. The IEEE 802.15.6 standard requires the phase error $< 11°$.

However, in order to reduce the phase error further, a fine delay adjustment scheme is used. It is achieved through independent tunable resistive degeneration of the inverters and gates in the $LO$ and $\overline{LO}$. This finely adjusts the delay of the gate, and the final implementation achieves overall $\pm 12°$ phase tuning in steps of 1–2°.

## V. Integrated Pulse-Shaping Power Amplifier

The power amplifier must be optimized for high efficiency at an output power of $-10$ dBm, while operating from a 0.7 V power supply. On a single-ended 50 Ω antenna, this amounts to a swing of 200 $\text{mV}_{\text{p-p}}$. An impedance transformation network is therefore necessary for a high-efficiency power amplifier. The rest of the section describes the choice of topology, device sizing, impedance transformation network type, biasing and pulse-shaping capability.

### A. NMOS-Only versus Push-Pull Topology

Fig. 7(a) shows a typical NMOS-only power amplifier topology. The choke inductor could be replaced by a smaller inductor that is part of the matching network [6]. Rather than using it as a linear power amplifier with output proportional to the input, it is driven strongly by the rail-to-rail swinging output of the resonant buffer for maximum efficiency operation. In this mode of operation, the drain node has a swing of $2V_{DD}$. If $R_L$ is the impedance provided by the matching network, the output power is given by

$$P_{\text{out,max}} = \frac{V_{DD}^2}{2R_L}.$$

For the PA to operate at peak efficiency for $-10$ dBm, $R_L = 2.45$ kΩ. The required impedance transformation ratio of 50 is very high, and is not practical for on-chip implementations, with typical inductor-Q values less than 10 [19].

On the other hand, for the push-pull PA shown in Fig. 7(b) the drain node swings from 0 to only $V_{DD}$ when operating at its peak efficiency, thus effectively reducing the output power delivered for the same load impedance. The output power is given by

$$P_{\text{out,max}} = \frac{V_{DD}^2}{8R_L}. \tag{6}$$

Hence, for $-10$ dBm output, $R_L = 612$ Ω. This impedance transformation ratio of 12 is amenable to on-chip implementations.

Typically, power amplifiers also include a series LC network resonant at the center frequency in order to provide dc-blocking, filter harmonics and improve efficiency. But, in a high-impedance system with a 612 Ω load, the parasitic capacitance of the inductor can provide a lower impedance path, affecting the overall efficiency. For example, 100 fF at 2.5 GHz is an impedance of $-j600$ Ω. The series LC filter is hence replaced with a DC-blocking capacitor.

### B. Tunable Impedance Transformation Networks

Once the supply voltage and load impedance are fixed, the power amplifier has a constant output power given by (6). In order to change the output power, either the supply voltage or the effective impedance seen by the PA must be changed. For pulse shaping using the former method, a supply modulator would be required. Since 1 Mbps data rates are considered, the bandwidth of the supply modulator would need to greater than 1 MHz. Class-S supply modulators are ideally 100% efficient [20], however, the use of external components and the overhead of the control circuits and other losses can be prohibitive, especially for low output power applications.

An alternate method of adjusting the effective impedance provided to the PA is explored in this work. For this, a tunable impedance transformation network is designed. The network must achieve resonance at multiple settings, while transforming the impedance to different values. The settings of the network are to be made digitally tunable in order to enable streamlined pulse shaping. At each of the settings, the PA operates at its peak efficiency, with the drain swinging rail-to-rail. Amplitude modulation is achieved even with a constant envelope input, thus simplifying the design of the previous stages.

Since on-chip inductors are low-Q and have a large area, it is undesirable to add switches in series with the inductor in order to select from a set of inductor values. Thus, fixed-inductor designs are explored. This eliminates the a simple L-match since a fixed valued inductor can only provide a fixed impedance transformation. Similarly, matching networks with two inductors are avoided because of the increased area. Thus, a pi-matching network and a tapped-capacitor matching network are considered and shown in Fig. 8.

The design equations for the tapped capacitor match are given below, derived through narrow-band parallel-to-series transformations [19]:

$$Q_2 = \omega \cdot C_2 \cdot 50 \tag{7}$$

$$C_{2,\text{s}} = C_2 \cdot \frac{(Q_2^2+1)}{Q_2^2}, \quad R_{\text{s}} = \frac{50}{Q_2^2+1} \tag{8}$$

$$C_{\text{s,eff}} = \frac{C_1 C_{2,\text{s}}}{C_1 + C_{2,\text{s}}}, \quad Q_L = \frac{1}{\omega \cdot C_{\text{s,eff}} \cdot R_{\text{s}}} \tag{9}$$

$$C_{\text{eff}} = C_{\text{s,eff}} \cdot \frac{Q_L^2}{Q_L^2+1}, \quad R_L = R_{\text{s}} \cdot (Q_L^2+1) \tag{10}$$

$$\omega^2 = \frac{1}{LC_{\text{eff}}}. \tag{11}$$

$Q_2$ is the loaded quality factor of the capacitor $C_2$, $R_{\text{s}}$ is the series impedance seen by the effective series capacitance, $C_{\text{s,eff}}$ formed by $C_1$ and $C_2$. $Q_L$ is the loaded quality factor of this effective series capacitance, and also the loaded quality factor of the inductance. Thus, for a desired value of $R_L$, the required values of $C_1$ and $C_2$ can be calculated. A similar analysis can be done for the pi-match.

Since the analysis above assumes ideal passives, the "loaded quality factor" indicates the ratio of energy stored in the element to the energy radiated by the antenna per cycle [19].

TABLE I
DESIGN OF TAPPED CAPACITOR MATCH FOR VARIABLE IMPEDANCES, AT 2.5 GHz

| $L(nH)$ | $C_1(fF)$ | $C_2(fF)$ | $R_L(\Omega)$ | $Q_L$ |
|---|---|---|---|---|
| 6.44 | 958 | 1012 | 300 | 3 |
| | 890 | 1460 | 450 | 5.4 |
| | 851 | 1807 | 600 | 7.1 |
| | 805 | 2366 | 900 | 9.7 |
| | 779 | 2820 | 1200 | 11.9 |

TABLE II
DESIGN OF $\pi$-MATCH FOR VARIABLE IMPEDANCES, AT 2.5 GHz

| $L(nH)$ | $C_1(fF)$ | $C_2(fF)$ | $R_L(\Omega)$ | $Q_L$ |
|---|---|---|---|---|
| 6.44 | 774 | 1498 | 300 | 4.8 |
| | 784 | 2024 | 450 | 7.2 |
| | 777 | 2399 | 600 | 9.2 |
| | 760 | 2977 | 900 | 13.2 |
| | 746 | 3438 | 1200 | 16.8 |

But, in reality, the passives have a finite intrinsic quality factor ($Q_{\text{intrinsic}} = \omega L/R_{\text{ind,parasitic}}$ or $1/\omega C R_{cap,\text{parasitic}}$), which implies that a fraction of the stored energy is also dissipated by these losses every cycle. The power loss in a passive is:

$$P_{\text{loss}} = P_{\text{out}} \cdot \frac{Q_{\text{loaded}}}{Q_{\text{intrinsic}}}. \tag{12}$$

This indicates that for a given intrinsic $Q$, the efficiency of the matching network reduces as the loaded $Q$ seen by the passive element increases. Thus, matching networks that minimize loaded $Q$ are more preferable.

The results for the two matching networks using a fixed 6.44 nH on-chip inductor are shown in Tables I and II for impedance transformation from 300 Ω to 1.2 kΩ. The capacitance tuning required is similar in both the cases. However, the loaded Q of the inductor in the pi-match is larger, leading to higher matching network losses. Fig. 9 plots the phase of the RF signal at the antenna relative to the phase of the RF input into the PA. The variation of this phase difference for the pi-matching network is much higher as compared to the tapped-capacitor one, and is therefore once again the more undesirable topology. Hence, the tapped-capacitor match is chosen for this design. It should be noted that even at the highest $Q_L$ of 12 in the tapped capacitor match, the network has a bandwidth ≈ 200 MHz, and hence, for each impedance transformation ratio, a single capacitor bank setting is sufficient over the entire ISM band.

### C. Design of Capacitor Banks

The capacitor banks $C_1$ and $C_2$ require a wide tuning of about 2–3×, while also maintaining a high Q. They are designed with some fixed capacitance and a binary-weighted capacitor bank built with MIM-capacitors. A 5-bit capacitor bank is designed for $C_1 \cdot C_2$ is designed with 7 bits since it requires a larger range of values. The bottom plates of both the capacitors see a DC voltage of 0 V due to the 50 Ω antenna. Also, since the voltage swing is a few hundred mVs, the bank design is identical for both and is presented below. Fig. 10(a) shows a capacitor with a switch and its parasitics. $C_{\text{par2}} = C_{\text{bottom2}}$, $C_{\text{par}} = C_{\text{bottom}} + C_{\text{ds}}$, which are dependent on the capacitor value and switch size. The switch is sized based on the equations below:

$$C_{\text{Switch ON}} \approx C + C_{\text{par2}} \tag{13}$$

$$C_{\text{Switch OFF}} \approx C_{\text{par}} + C_{\text{par2}} \tag{14}$$

$$Q_{\text{Switch ON}} \approx \frac{1}{\omega R_{\text{Switch}} C} \tag{15}$$

$$Q_{\text{Switch OFF}} \to \infty \tag{16}$$

$$C_{\text{Step}} = C - C_{\text{par}}. \tag{17}$$

$C_{\text{ds}}$ part of $C_{\text{par}}$ also scales with $C$ if the switch size is scaled along with it. This leads to a constant-Q switched capacitor. The off-state capacitance is $C_{\text{par}}$ and adds to the explicit fixed capacitor. The effective $Q$ of the capacitor bank is thus highest at small digital codes and degrades at higher digital codes.

In order to generate a wide tuned capacitor, $C_{\text{ds}}$ must be minimized for a given switch resistance since it contributes to the fixed capacitance. A boosted voltage of 1 V is hence used to drive the switches, allowing smaller switches to be used. Fig. 10(b) shows the simulated capacitance and $Q$ for $C_1$, with $C_2$ being quite similar. These capacitor banks, being digitally switched, can be changed at rates > 10 MHz, sufficient for up to 10× oversampled pulse shaping of 1 Mbps OOK and BPSK modulations.

In this work, the logic for driving the capacitor banks to apply pulse-shaping is implemented off-chip on an FPGA, as indicated in Fig. 3 and Section II. However, it is important to estimate the power overhead of this operation. In [7], the digital baseband including packet generation and raised-cosine pulse-shaping consumes only 62 $\mu$W. Based on this and power scaling in digital circuits [21], the pulse shaping logic required for this work is estimated to result in less than 2% degradation in overall system efficiency for −10 dBm operation.

### D. Final PA Design

The final design of the proposed push-pull PA is illustrated in Fig. 11. Transistors M1 and M2 are biased at ≈ $V_{TN}$ and ≈ $(V_{DD} + V_{TP})$ respectively with on-chip DACs to trade-off short-circuit current and on-resistance. This is done to make the most use of the 0.7 V swing from the resonant buffer. Resistive-divider DACs, designed with high-density poly resistors, have a total resistance of 1 MΩ leading to a power consumption of < 2 $\mu$W. The DACs do not need to drive strongly since they are set only once and not changed at the data rate.

An ac-coupling capacitor connects the drain node $D$ of the PA to the tapped-capacitor matching network. Though a series resonant LC tank could be used instead to improve efficiency by presenting a high-impedance at the higher harmonics [19], capacitive parasitics of the on-chip inductor would create shunt paths due to the high impedance of the subsequent matching network (as described in Section V-A).

The biasing resistor $R_{\text{bias}}$ sets the DC voltage on the transistors, while a coupling capacitor connects the RF from the resonant buffer. The coupling capacitor and gate capacitance forms a voltage divider, and the bias resistor acts as an additional load impedance to the resonant buffer. The coupling capacitor is sized to keep the voltage division close to 1.

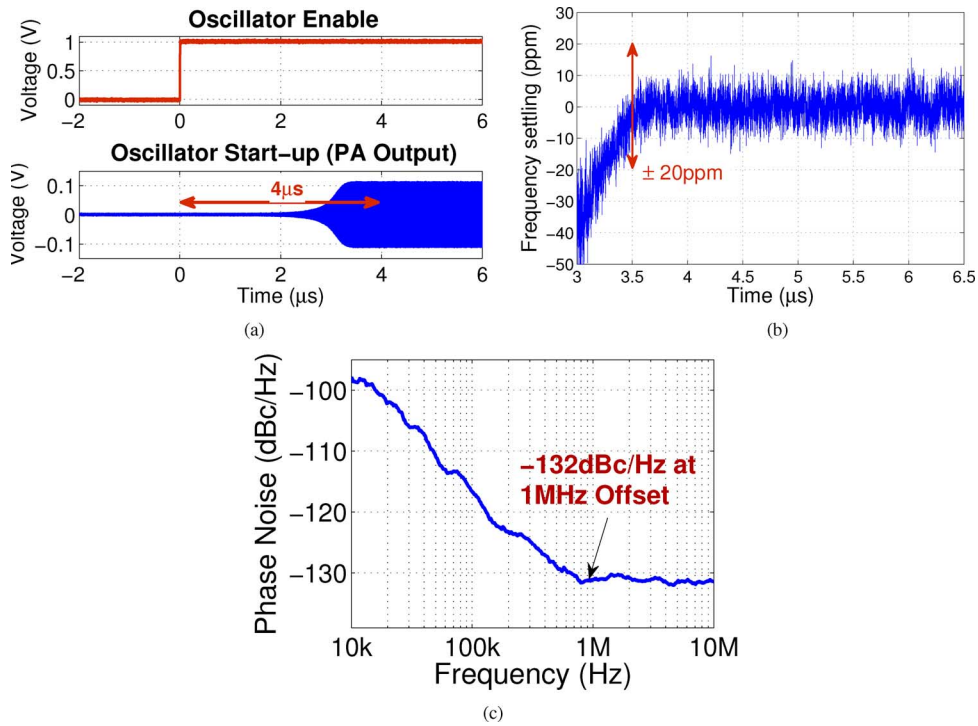



Fig. 13. Measurement results of FBAR oscillator. (a) Startup time. (b) Frequency settling transient. (c) Phase noise measured at the output of the transmitter.

A total of 7.5 dB output power tuning range is achieved in the final design through the tunable impedance transformation network by implementing a slightly wider capacitance tuning range as compared to Table I. Further tuning of output power, if required, can be achieved by statically varying the supply voltage of the PA alone through high-efficiency DC-DC converters. Hence, in the most flexible system, a DC-DC converter sets the average power of the transmitter while the pulse shaping is provided by the matching network.

## VI. Measurement Results

The transmitter is fabricated in a 65 nm CMOS process and is co-packaged with three FBARs in a 40-pin QFN package, as shown in the package and chip photographs in Fig. 12. The TX core occupies an area of 0.324 mm$^2$. All the RF circuits are nominally powered from a 0.7 V supply, while the digital switches in the multiplexers and capacitor banks are powered with a 1 V supply. An FPGA is used to configure the serial interface of the chip, and to provide data and pulse shaping information. The measurements are done using a Agilent MXA N9020A Spectrum Analyzer and a Agilent DSO90254A Digital Storage Oscilloscope.

### A. Oscillators

Each FBAR oscillator consumes 150 $\mu$W. The center frequencies of the three channels as defined by the FBARs in one of the measured chips are at 2.421 GHz, 2.480 GHz and 2.491 GHz, as shown in Fig. 16. Through the capacitor bank, $C_{\mathrm{MSK}}$, the oscillator center frequency can be tuned over a 600 kHz range with a 9.5 kHz step-size. The intrinsic phase noise of the oscillator is not measurable in this design. However, the phase noise at the output of the transmitter PA is measured, and plotted in Fig. 13(c). At a 1 MHz offset, the phase noise is measured to be $-132$ dBc/Hz.

After the oscillator enable signal is turned on, the RF output at the antenna stabilizes in under 4 $\mu$s as shown in Fig. 13(a).

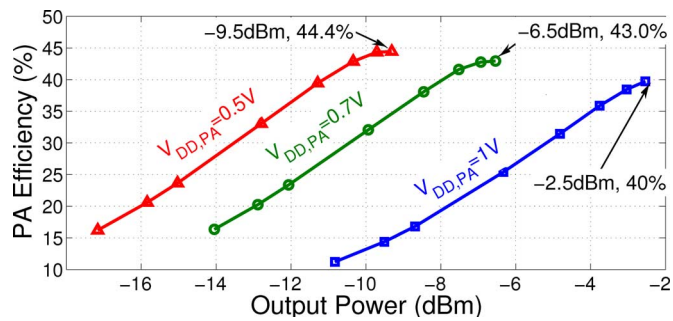



Fig. 14. Efficiency of the PA for various $V_{DD,\mathrm{PA}}$ and impedance transformation settings.

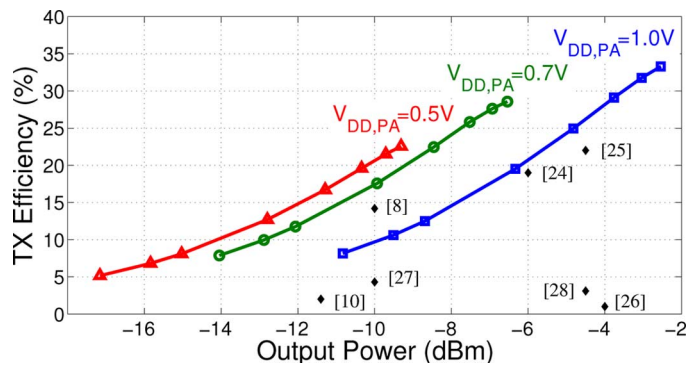



Fig. 15. Overall efficiency of the transmitter plotted for various $V_{DD,\mathrm{PA}}$ and impedance transformation settings. Results are also compared to previous frequency-stable TXs.

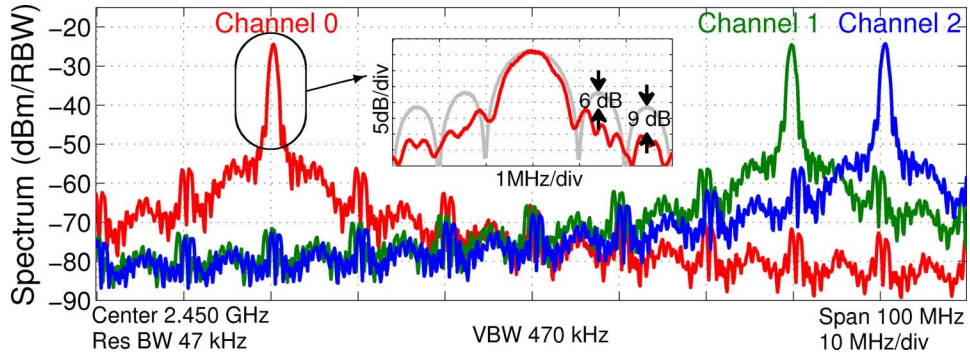



Fig. 16. Spectra of Gaussian pulse-shaped and phase-scrambled 1 Mb/s OOK for the three channels measured from the chip.

The Frequency accuracy at 4 $\mu$s is better than $\pm 20$ ppm. The startup time corresponds to only 4 bit periods, ensuring efficient operation of the transmitter for even very short-length packets.

### B. Power Amplifier

The power amplifier is characterized for a nominal supply voltage of 0.7 V as well as for 0.5 V and 1 V. When the PA supply voltage is changed, the rest of the circuits are still operated at 0.7 V. At each PA supply voltage, the DAC voltages are re-adjusted to optimize the short-circuit current versus on-resistance trade-off. The bias voltages and currents in the oscillator and buffer circuits are not changed. The output power is swept only by varying the impedance transformation network setting.

Fig. 14 shows the efficiency of the PA alone. At 0.7 V, the output power tuning is centered around $-10$ dBm and the peak PA efficiency is 43% for an output power of $-7$ dBm. At 0.5 V, the peak efficiency increases to 44.4% at $-9.5$ dBm output power and at 1 V, the peak efficiency goes to 40% for $-2.5$ dBm.[1] The peak efficiencies remain approximately constant since the losses in the tank and switches scale with the square of supply voltage, which is the same as the scaling of output power with supply. Overall, with supply voltage adjustment and the tunable impedance transformation network, the PA achieves 14.5 dB tuning range from $-17$ dBm up to $-2.5$ dBm.

In Fig. 15, the overall efficiency is plotted as the ratio of radiated power to power consumption of the entire transmitter. At 0.7 V PA supply, peak TX efficiency is 28.6%. At 1 V PA supply, it increases to 33%, while at 0.5 V, it drops to 23%. Unlike the PA efficiency, the peak transmitter efficiency does not remain constant at each PA supply voltage because of the constant fixed power consumed by the oscillators and buffer stages.

The figure also compares the transmitter to other frequency-stable transmitters with sub-mW outputs operating at GHz frequencies. This work has the highest transmitter efficiency at each of the output power values considered. For the moderate data rates and simple modulation schemes considered in similar designs, this metric is a fair comparison because it eliminates other variables like the data rate and range of the communication.

[1]With the supply voltage increased to 1 V, the peak output power increased by 4 dB instead of the expected 3 dB. This is attributed to a change in PA bias voltages which are adjusted to re-optimize short-circuit current and on-resistance.

### C. Modulation and Pulse Shaping

*1) OOK With Gaussian Pulse Shaping:* OOK modulation is first considered. Gaussian pulse shaping with $\alpha = 0.3$ is used with an over-sampling rate of $10\times$. The spectrum of OOK data has a feed-through component, which results in a spur at the center frequency. When the pulse-shaping is done through the switches, this spur is also modulated to the harmonics of the $10\times$ switching frequencies. This is undesirable, since it falls in the adjacent channels.

In order to avoid this, the data is also phase-scrambled through the BPSK path in the buffer with a pseudo-random sequence [17], thus eliminating the spurs. The phase-scrambling, however, causes a reduction in the average output power since the instantaneous power goes to 0 during phase transitions. Fig. 16 shows the superimposed spectra for 1 Mbps OOK of the three channels measured on the chip. This shows the multi-channel capability of the architecture. Spurs from the $10\times$ oversampling are all below $-30$ dBc. A zoomed-in version of the spectrum is shown in the inset, comparing it to the no-pulse-shaping case. Pulse-shaping reduces the first sidelobe by 6 dB and the second sidelobe by 9 dB.

Fig. 17 shows the time domain waveform of the pulse-shaped OOK data, with the phase scrambling instances marked. Overall, for a $-12.5$ dBm average output power, the entire transmitter consumes 440 pJ/bit.

*2) BPSK With SRRC Pulse Shaping:* Square Root Raised Cosine (SRRC) pulse shaping with $\beta = 0.3$ and oversampling of $8\times$ is used for BPSK modulation. The first side-lobe is reduced by 13 dB, effectively reducing the $-20$ dBc bandwidth of the signal from 6 MHz down to only 1.5 MHz. Fig. 18 shows the time-domain and frequency spectra. The transmitter consumes 530 pJ/bit at 1 Mbps while transmitting an average of $-11$ dBm output power in this mode.

A Vector Signal Analyzer (VSA) is used to measure the modulation characteristics of the transmitter while sending random data. The rms phase error is 4.36° for 1 Mbps BPSK without pulse shaping. When the SRRC pulse shaping is applied, the rms phase error is 5.3°. This shows the reliable phase modulation and pulse shaping capability of the TX.

*3) MSK With Gaussian Pulse Shaping:* 1 Mbps GMSK modulation requires a frequency deviation of $\pm 250$ kHz. The Gaussian pulse shaping ($10\times$ oversampled) is applied to the tuning capacitor banks of the oscillators. As shown in Fig. 19,

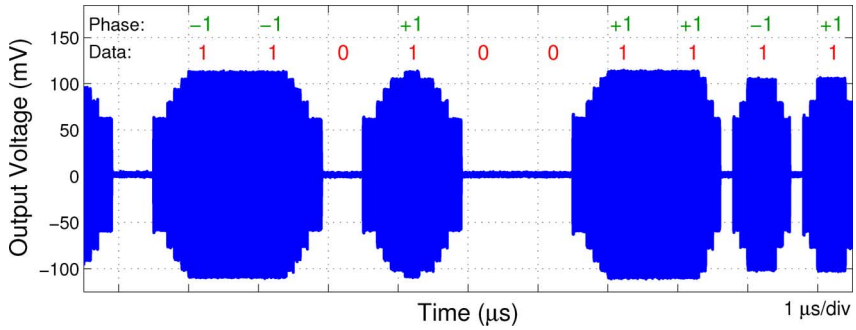



Fig. 17. 1 Mb/s OOK modulated waveform with Gaussian pulse shaping and phase scrambling.

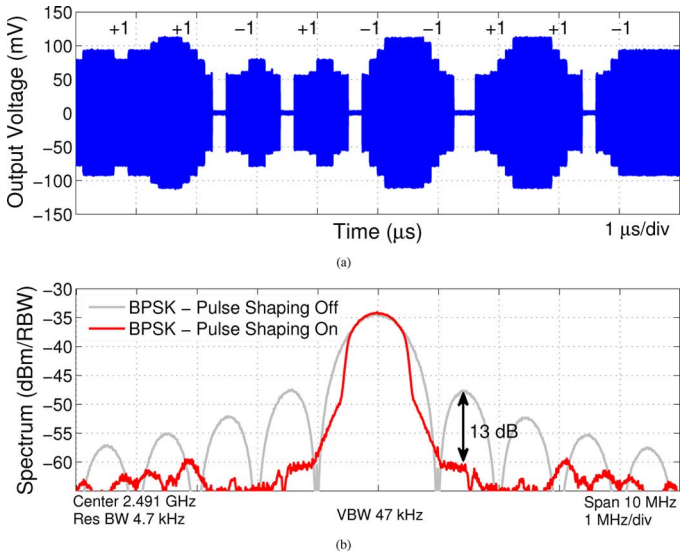



Fig. 18. 1 Mb/s BPSK with SRRC filtering. (a) 1 Mb/s BPSK modulated waveform with SRRC filtering. (b) 1 Mb/s BPSK spectra with and without pulse-shaping.

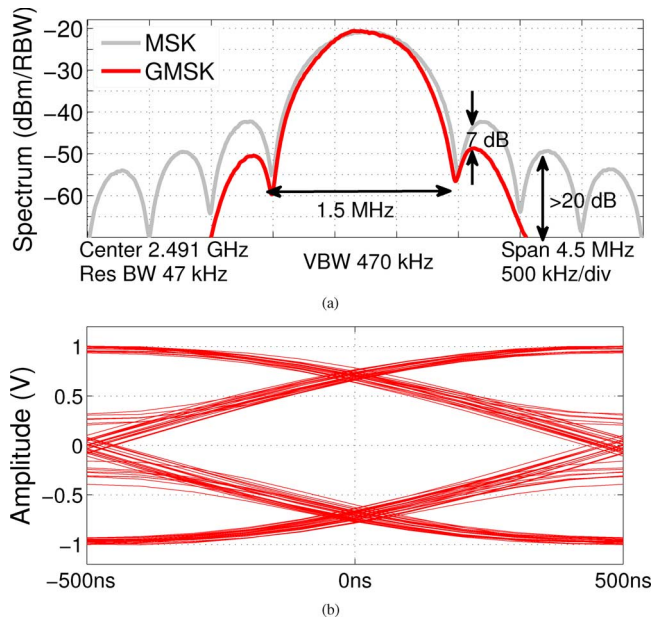



Fig. 19. 1 Mb/s GMSK. (a) Spectrum compared to MSK. (b) Eye diagram.

the pulse shaping reduced the first sidelobe by 7 dB and the second sidelobe by $>20$ dB as compared plain MSK. In this mode, the TX consumes 550 pJ/bit while delivering $-10$ dBm output power.

The Error Vector Magnitude (EVM) for MSK modulation is measured on a VSA to be 2.14% rms. For GMSK modulation, the EVM is 5.94%. Fig. 19(b) shows the 1 Mbps GMSK eye diagram as measured by the VSA, illustrating a wide eye.

### *D. Measurement Summary and Comparison*

The performance of the chip is summarized in Table III. Fig. 20 plots an important metric of comparison, the energy-per-bit versus the output power of previous low power transmitter designs. The data rate of each design is annotated.

It can be noted that some of the resonator-based transmitters have had much higher energy-per-bit, while the overall efficiency is favorable in many cases. This is because most of the systems that used the resonators have implemented relatively high output powers ($>-5$ dBm) and low data rates ($<330$ kbps) for achieving long distance communication, as opposed to the 1–2m Body Area Network scenario considered in this work.

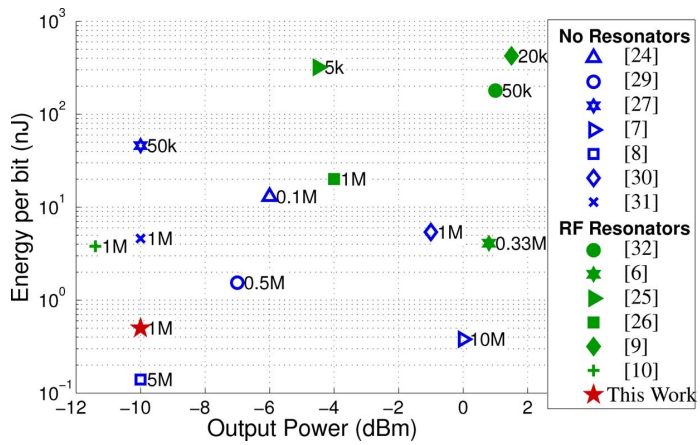



Fig. 20. Energy-per-bit versus output power for ultra-low power TXs, with data rate annotated.

The transmitter has also been used to successfully send packetized ECG data to a commercial receiver, TI's CC2500 [22]. The packet structure of the CC2500 including the preamble, sync word and FEC are implemented on the FPGA driving the transmitter.

TABLE III
TRANSMITTER PERFORMANCE SUMMARY

| | |
|---|---|
| Technology | 65 nm CMOS |
| Supply | 0.7 V (RF), 1 V(Switch) |
| Num. Channels | 3 |
| Startup Time | $4\ \mu s$ |
| Data Rate | 1 Mb/s |
| Phase Noise | -132 dBc/Hz (1 MHz off.) |
| PA Peak Eff. | 44.4% |
| TX Peak Eff. | 33% |
| $P_{OUT}$ | -17 dBm to -2.5 dBm |
| Energy per bit and Average $P_{OUT}$ | |
| OOK (Gauss.) | 440 pJ/bit at -12.5 dBm |
| BPSK(SRRC) | 530 pJ/bit at -11 dBm |
| GMSK | 550 pJ/bit at -10 dBm |

## VII. CONCLUSION

A transmitter architecture optimized for the short-distance link budgets of Body Area Networks has been presented. Specifically, the power amplifier has been optimized for operation at $-10$ dBm, and the tunable impedance transformation network results in efficient integrated pulse shaping, achieving high spectral efficiency. Further, high transmitter efficiency is achieved at these low output power levels by the use of a high-Q FBAR-based LO generation scheme. Multi-channel operation has been achieved using inherently single-channel resonators through efficient oscillator multiplexing. Future development of integrated on-chip resonators [23] will enable area-efficient expansion of this architecture to a larger number of channels. In addition, low voltage operation at 0.7 V and maximum use of the swing available at all RF nodes improves energy efficiency. Overall, the transmitter has been measured to consume 440 pJ/b for 1 Mbps Gaussian pulse-shaped OOK at an average output power of $-12.5$ dBm.

## ACKNOWLEDGMENT

Chip fabrication was done through the TSMC University Shuttle Program and FBARs were provided by Avago Technologies. The authors would like to thank S. Bandyopadhyay, M. Qazi, and B. Ginsburg for useful discussion and feedback.

## REFERENCES

[1] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, 2010.

[2] *IEEE Standard for Local and Metropolitan Area Networks Part 15.6: Wireless Body Area Networks*, , 2012, IEEE Std 802.15.6-2012.

[3] E. Reusens, W. Joseph, B. Latré, B. Braem, G. Vermeeren, E. Tanghe, L. Martens, I. Moerman, and C. Blondia, "Characterization of on-body communication channel and energy efficient topology design for wireless body area networks," *IEEE Trans. Inform. Technol. Biomed.*, vol. 13, no. 6, pp. 933–945, 2009.

[4] C. Cojocaru *et al.*, "A 43 mw Bluetooth transceiver with-91 dbm sensitivity," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2003, pp. 90–480.

[5] J. Bohorquez, A. Chandrakasan, and J. Dawson, "A 350 $\mu$W CMOS MSK transmitter and 400 $\mu$W OOK super-regenerative receiver for medical implant communications," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1248–1259, 2009.

[6] Y. Chee, A. Niknejad, and J. Rabaey, "A 46% efficient 0.8 dbm transmitter for wireless sensor networks," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2006, pp. 43–44.

[7] M. Vidojkovic *et al.*, "A 2.4 GHz ULP OOK single-chip transceiver for healthcare applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2011, pp. 458–460.

[8] J. Bae, L. Yan, and H. Yoo, "A low energy injection-locked FSK transceiver with frequency-to-amplitude conversion for body sensor applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 928–937, 2011.

[9] B. Otis, Y. Chee, R. Lu, N. Pletcher, and J. Rabaey, "An ultra-low power mems-based two-channel transceiver for wireless sensor networks," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2004, pp. 20–23.

[10] D. Daly and A. Chandrakasan, "An energy-efficient OOK transceiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1003–1011, 2007.

[11] B. Otis *et al.*, "A 300 $\mu$W 1.9-GHz CMOS oscillator utilizing micromachined resonators," *IEEE J. Solid-State Circuits*, 2003.

[12] A. Paidimarri, P. Nadeau, P. Mercier, and A. Chandrakasan, "A 440 pJ/bit 1 Mb/s 2.4 GHz multi-channel FBAR-based TX and an integrated pulse-shaping PA," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 34–35.

[13] Y. Chee, A. Niknejad, and J. Rabaey, "A sub-100 $\mu$W 1.9-GHz CMOS oscillator using FBAR resonator," in *IEEE RFIC Symp. Dig. Papers*, 2005, pp. 123–126.

[14] E. Vittoz, M. Degrauwe, and S. Bitz, "High-performance crystal oscillator circuits: Theory and application," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 774–783, 1988.

[15] N. Nguyen and R. Meyer, "Start-up and frequency stability in high-frequency oscillators," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, pp. 810–820, 1992.

[16] S. Chan, P. Restle, K. Shepard, N. James, and R. Franch, "A 4.6 GHz resonant global clock distribution network," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2004, vol. 1, pp. 342–343.

[17] P. Mercier, D. Daly, and A. Chandrakasan, "An energy-efficient all-digital uwb transmitter employing dual capacitively-coupled pulse-shaping drivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1679–1688, 2009.

[18] B. Razavi, K. Lee, and R. Yan, "A 13.4-GHz CMOS frequency divider," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 1994, pp. 176–177.

[19] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Second ed. Cambridge, U.K.: Cambridge Univ Press, 2004.

[20] F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, and N. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 814–826, 2002.

[21] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*. Englewood Cliffs, NJ, USA: Prentice-Hall, 2002.

[22] Low-Cost Low-Power 2.4 GHz RF Transceiver, CC2500 Datasheet. Texas Instruments. [Online]. Available: http://focus.ti.com/lit/ds/symlink/cc2500.pdf

[23] D. Weinstein and S. A. Bhave, "The resonant body transistor," *Nano Lett.*, vol. 10, no. 4, pp. 1234–1237, Apr. 2010.

[24] A. Molnar, B. Lu, S. Lanzisera, B. Cook, and K. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2004, pp. 401–404.

[25] B. Otis, Y. Chee, and J. Rabaey, "A 400 $\mu$W-RX, 1.6 mW-TX super-regenerative transceiver for wireless sensor networks," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2005, vol. 1, pp. 396–606.

[26] D. Ruffieux, J. Chabloz, M. Contaldo, C. Muller, F. Pengg, P. Tortori, A. Vouilloz, P. Volet, and C. Enz, "A narrowband multi-channel 2.4 GHz mems-based transceiver," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 228–239, 2009.

[27] A. Wong, D. McDonagh, G. Kathiresan, O. Omeni, O. El-Jamaly, T. Chan, P. Paddan, and A. Burdett, "A 1 v, micropower system-on-chip for vital-sign monitoring in wireless body sensor networks," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2008, pp. 138–602.

[28] P. Bradley, "An ultra low power, high performance medical implant communication system (mics) transceiver for implantable devices," in *Proc. IEEE Biomed. Circuits and Syst. Conf.*, 2006, pp. 158–161.

[29] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.
[30] Y.-H. Liu, X. Huang, M. Vidojkovic, K. Imamura, P. Harpe, G. Dolmans, and H. De Groot, "A 2.7 nj/b multi-standard 2.3/2.4 GHz polar transmitter for wireless sensor networks," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 448–450.
[31] A. Wong, M. Dawkins, G. Devita, N. Kasparidis, A. Katsiamis, O. King, F. Lauria, J. Schiff, and A. Burdett, "A 1 v 5 ma multimode ieee 802.15.6/Bluetooth low-energy wban transceiver for biotelemetry applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 300–302.
[32] M. Flatscher, M. Dielacher, T. Herndl, T. Lentsch, R. Matischek, J. Prainsack, W. Pribyl, H. Theuss, and W. Weber, "A robust wireless sensor node for in-tire-pressure monitoring," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 286–287.

**Arun Paidimarri** (S'10) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 2009 and the S.M. degree in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2011, where he is currently pursuing the Ph.D. degree.

From June 2011 to August 2011, he worked in the Low Power RF division in Texas Instruments, Dallas, TX, USA, designing low power timer circuits. From June 2012 to August 2012, he worked on low power PAs at Kilby Labs in Texas Instruments, Dallas, TX. His research interests include low power RF circuits and systems design.

Mr. Paidimarri was awarded the President of India Gold Medal in 2009. He was a Silver Medal winner at the 37th International Chemistry Olympiad held in Taipei, Taiwan, in 2005.

**Phillip M. Nadeau** (S'10) received the B.A.Sc. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 2009, where he received the Governor General's Academic Silver Medal. He subsequently received the S.M. degree in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2011, where he is currently pursuing the Ph.D. degree. His research interests are in ultra-low-power IC design for biomedical applications.

From June 2012 until August 2012 he worked in Texas Instruments' Kilby Labs in Dallas, TX, USA, on mm-wave circuits and systems. From June 2011 until August 2011 he was with the Radio Integration Research Lab at Intel in Hillsboro, OR, USA, working on low power timer circuits.

Mr. Nadeau received Natural Sciences and Engineering Council of Canada fellowships in 2009 and 2012. He also received the Harold L. Hazen Teaching award from MIT in 2012.

**Patrick P. Mercier** (S'04–M'12) received the B.Sc. degree in electrical and computer engineering from the University of Alberta, Edmonton, AB, Canada, in 2006, and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 2008 and 2012, respectively.

He is currently an Assistant Professor at the University of California at San Diego, La Jolla, CA, USA, in the Department of Electrical and Computer Engineering. His research interests include the design of energy-efficient digital systems, RF circuits, power converters, and sensor interfaces for biomedical and implantable applications.

Prof. Mercier was a co-recipient of the 2009 ISSCC Jack Kilby Award for Outstanding Student Paper at ISSCC 2010. He also received a Natural Sciences and Engineering Council of Canada (NSERC) Julie Payette fellowship in 2006, NSERC Postgraduate Scholarships in 2007 and 2009, and an Intel Ph.D. Fellowship in 2009.

**Anantha P. Chandrakasan** (M'95–SM'01–F'04) received the B.S, M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1989, 1990, and 1994, respectively.

Since September 1994, he has been with the Massachusetts Institute of Technology, Cambridge, where he is currently the Joseph F. and Nancy P. Keithley Professor of Electrical Engineering.

He was a co-recipient of several awards including the 1993 IEEE Communications Society's Best Tutorial Paper Award, the IEEE Electron Devices Society's 1997 Paul Rappaport Award for the Best Paper in an EDS publication during 1997, the 1999 DAC Design Contest Award, the 2004 DAC/ISSCC Student Design Contest Award, the 2007 ISSCC Beatrice Winner Award for Editorial Excellence and the ISSCC Jack Kilby Award for Outstanding Student Paper (2007, 2008, 2009). He received the 2009 Semiconductor Industry Association (SIA) University Researcher Award. He is the recipient of the 2013 IEEE Donald O. Pederson Award in Solid-State Circuits.

His research interests include micro-power digital and mixed-signal integrated circuit design, wireless microsensor system design, portable multimedia devices, energy efficient radios and emerging technologies. He is a co-author of *Low Power Digital CMOS Design* (Kluwer Academic Publishers, 1995), *Digital Integrated Circuits* (Pearson Prentice-Hall, 2003, 2nd edition), and *Sub-threshold Design for Ultra-Low Power Systems* (Springer 2006). He is also a co-editor of *Low Power CMOS Design* (IEEE Press, 1998), *Design of High-Performance Microprocessor Circuits* (IEEE Press, 2000), and *Leakage in Nanometer CMOS Technologies* (Springer, 2005).

He has served as a technical program co-chair for the 1997 International Symposium on Low Power Electronics and Design (ISLPED), VLSI Design '98, and the 1998 IEEE Workshop on Signal Processing Systems. He was the Signal Processing Sub-committee Chair for ISSCC 1999–2001, the Program Vice-Chair for ISSCC 2002, the Program Chair for ISSCC 2003, the Technology Directions Sub-committee Chair for ISSCC 2004–2009, and the Conference Chair for ISSCC 2010–2012. He is the Conference Chair for ISSCC 2013. He was an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1998 to 2001. He served on SSCS AdCom from 2000 to 2007 and he was the meetings committee chair from 2004 to 2007. He was the Director of the MIT Microsystems Technology Laboratories from 2006 to 2011. Since July 2011, he is the Head of the MIT EECS Department.