A 78%- Efficiency Li-ion- Compatible Fully-Integrated Modified 4-Level Converter with 0.01- 40mW DCM- Operation in 28nm FDSOI

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La Jolla, CA, USA
Powering IoT and Wearables in Scaled-CMOS

Small wearable/IoT devices is implemented in scaled-CMOS and use Li-ion batteries as power supply.
Powering IoT and Wearables in Scaled-CMOS

Conventional

Power Management IC

- ≥180nm Chip
  - High-V transistor available

LDO

- 0.6-1V

Wearable/IoT Chip

- ≤28nm Chip

- Sensors
- Process
- RF Tx/Rx

Discrete PMIC is implemented in technologies that can handle the high battery voltage

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Powering IoT and Wearables inScaled-CMOS

Conventional

- Power Management IC
  - Bulky L, high-Q
  - 2.8-4.2V input
  - 1.8V output
  - ≥180nm Chip
  - High-V transistor available

- Wearable/IoT Chip
  - LDO
  - 0.6-1V output
  - Sensors
  - RF Tx/Rx
  - ≤28nm Chip

↑ Area  ↑ PCB complexity/cost
Powering IoT and Wearables in Scaled-CMOS

**Conventional**

- **Power Management IC**
  - ≥180nm Chip
  - High-V transistor available
  - Bulky L, high-Q
  - 2.8-4.2V

- **Wearable/IoT Chip**
  - ≤28nm Chip
  - 0.6-1V

- **Sensors**
- **Process**
- **RF Tx/Rx**

- **LDO**

**Goal**

- **Wearable/IoT Chip**
  - ≤28nm Chip
  - Only Low-V transistor available
  - 2.8-4.2V

- **PMU***

- **Sensors**
- **Process**
- **RF Tx/Rx**

**Area ↑ PCB complexity/cost**

**Small form factor**

**PMU***: Power Management Unit
Li-ion Fully-Integrated PMU Challenges in 28nm FDSOI

- High switching & conduction losses
- Complex power-hungry drivers
- Many level shifters

Scaled-CMOS Challenges

- Only Low-V transistors available
  - Transistors stacking required
  - High switching & conduction losses
  - Complex power-hungry drivers
  - Many level shifters

- Only Low-V capacitors available
  - Capacitors stacking required
  - Large area
  - Low power density

- Poor quality on-chip passives
  - Large ESR, parasitic cap
  - Low density

- Only Low-V transistors available
- Only Low-V capacitors available

Low power density

Poor efficiency

- High conversion ratio
- Poor efficiency

High conversion ratio

3-4.2V Li-ion Battery
0.6-1V IoT & Wearables

Input PMU Output
Outline

- Prior Work
  - Proposed Hybrid Architecture
  - Switching Phases of the Proposed Architecture
  - Circuit Details
- Measurement Results
- Conclusion
Prior Work

- **Bulky L, high-Q**
  - ≥180nm Chip: High-V transistor available
  - ≤28nm Chip: Only Low-V transistor available
  - LDO: 0.6-1V
  - Buck

- **SC**
  - Wibben et al., JSSC'08
  - Souvignet et al., TPEL'16

- **Magnetic coupling**
  - Kumar et al., CICC'15

- **SoC**
  - ≥65nm Chip: High-V transistor available
  - ≥45nm Chip: Only Low-V transistor available
  - 2.8-4.2V

- **This work**
  - 28nm Chip: Only Low-V transistor available
  - PMU: 0.6-1V

- **Le et al., ISSCC'13**
- **Bang et al., JSSC’16**
- **Bandyopadhyay et al., JSSC’11**
Fully Integrated DC-DC Converter for $V_{in}=2.8-4.2V$

- **Buck**
  - Large ESR
  - Small L $\rightarrow$ high $F_{sw}$
  - Poor efficiency
  - $rs\approx 100\text{m}\Omega/\text{nH}$
  - Small L, Low Q

- **SC**
  - Charge sharing losses
  - High efficiency @ discrete ratios only
  - Low power density

- **Multi-Level**
  - Unlimited conversion ratios
  - No charge sharing losses
  - Low $F_{sw}$
  - High efficiency

**28nm Chip**

- Sensors
- Process
- RF
- Tx/Rx
Outline

- Prior Work
- Proposed Hybrid Architecture
  - Switching Phases of the Proposed Architecture
- Circuit Details
- Measurement Results
- Conclusion
Towards Fully-Integrated Li-ion PMU in Scaled CMOS

Starting point: Buck

2-Level Buck

\[ 2.8V \leq V_{\text{in}} \leq 4.2V \]

1.5V Transistor

\[ V_x: 0 \rightarrow V_{\text{in}} \]

Small on-chip L, large ESR
- High Switching & conduction losses
- Poor efficiency
Towards Fully-Integrated Li-ion PMU in Scaled CMOS

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Improving on-chip efficiency

Stacking transistors is required anyway
Towards Fully-Integrated Li-ion PMU in Scaled CMOS

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- Poor efficiency

Improving on-chip efficiency

4-Level Converter

\[ 2V_{\text{in}}/3 \]

Reduced swing at \( V_x \)

\[ F_{\text{sw}} \text{ reduced by } > 23x \]
\& efficiency by up to 33%

Stacking transistors is required anyway
Towards Fully-Integrated Li-ion PMU in Scaled CMOS

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\[ V_{in} \leq 4.2V \]

1.5V Transistor

\[ V_x: 0 \rightarrow V_{in} \]

Improving on-chip efficiency

4-Level Converter

\[ 2V_{in}/3 \]

\[ V_{in}/3 \]

\[ C_{f1} \]

\[ C_{f2} \]

\[ V_x: 0 \rightarrow V_{in}/3 \]

DCM-operated

Constant \( I_{pk} \)

Normalized Switching Frequency

\[ F_{sw-2L} \]

\[ F_{sw-4L} \]

\[ \frac{F_{sw-4L}}{F_{sw-2L}} = \frac{1/3 - V_{out}/V_{in}}{1 - V_{out}/V_{in}} \]

Small on-chip \( L \), large ESR

- High Switching & conduction losses
- Poor efficiency

Reduced swing at \( V_x \)

\( F_{sw} \) reduced by > 23x

& efficiency by up to 33%
The converter operates only in a single-mode for:

$$2.8 \leq V_{in} \leq 4.2 \& \ 0.6 \leq V_{out} \leq 1$$
Conventional 4-Level Converter Area Penalty

Conventional 4-Level

\[ V_{\text{max-MIM}} = 1.4V \]

\[ \frac{2V_{\text{in}}}{3} = 2.8V \]

\[ \frac{V_{\text{in}}}{3} \]

4 caps needed
Large area!
Low power density

Reducing cap area by 4x

Proposed Modified 4-Level

1 cap only
Reduce overstress

Changing the switching states of flying caps reduces the cap voltage stress
The overall efficiency is higher even with the added power switches because the proposed architecture allows larger passives for same area.
DCM-Operated Modified 4-Level Converter

DCM-operated architecture to achieve high efficiency @ low load current
DCM-Operated Modified 4-Level Converter

DCM-operated architecture to achieve high efficiency @ low load current

Ringing on $V_x$ in inductor zero current phase can go up to 2V

overstress transistor
DCM-Operated Modified 4-Level Converter

DCM-operated architecture to achieve high efficiency @ low load current

FW switches don’t contribute to losses:
1) Turn ON only in zero current phase (~no conduction losses)
2) Sized much less than other FETs

Eliminate ringing on $V_x$

1) Reliability
2) Improve efficiency by ~2%
Outline

- Prior Work
- Proposed Hybrid Architecture
  - Switching Phases of the Proposed Architecture
- Circuit details
- Measurement Results
- Conclusion
Converter Switching Cycle: 7 Inductor Phases

There are 7 different inductor switching phases in one converter switching cycle.

Capacitors steady state voltage:
\[ V_{f1} = V_{f2} = \frac{V_{in}}{3} \]

Gate signals in each phase set such that no transistor exceeds \( \frac{V_{in}}{3} \)
Converter Switching Cycle (7-phases)
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Converter Switching Cycle (7-phases)
Converter Switching Cycle (7-phases)

\[
\begin{align*}
\phi_3 & \quad \downarrow C_{f1} \quad 2V_{in}/3 \quad 2V_{in}/3 \\
\phi_2,4 & \quad \uparrow C_{f1} \quad \uparrow C_{f2} \quad \downarrow C_{f1} \quad \downarrow C_{f2} \\
V_x & \quad = \frac{V_{in}}{3} \\
V_{out} & \quad = \frac{V_{in}}{3}
\end{align*}
\]
Converter Switching Cycle (7-phases)

\[ \begin{align*}
\phi_1 & : C_f_1 \uparrow C_f_2 \\
\phi_2 & : V_x = V_{in}/3 \\
\phi_3 & : 2V_{in}/3 \\
\phi_4 & : V_x = 0
\end{align*} \]
Converter Switching Cycle (7-phases)

\[ \phi_5 \uparrow C_{f1} \uparrow C_{f2} \]

\[ \phi_2,4,6 \]

\[ \phi_{FW} \]

\[ V_{in} \]

\[ V_{in}/3 \]

\[ 2V_{in}/3 \]

\[ V_{out} \]

\[ 0 \]

\[ V_{out} \]

\[ V_{in}/3 \]

\[ 0 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ IL=0 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ 2V_{in}/3 \]

\[ V_{out} \]

\[ V_{x} = V_{in}/3 \]

\[ V_{x} = 0 \]

\[ V_{x} = V_{out} \]

\[ t \]

\[ IL \]

\[ V_{x} \]

\[ V_{in} \]

\[ T_{SW} \]

\[ V_{out} \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

\[ V_{in}/3 \]

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Power Stage 3-Level Gate Signaling

Challenge:
How to generate the 3-Level gate signals without complex stacked drivers and many level shifters?

3-Level gate signaling is required to ensure that none of the transistors exceed $V_{in}/3$.
Outline

- Prior Work
- Proposed Hybrid Architecture
- Switching Phases of the Proposed Architecture
- Circuit Details
- Measurement Results
- Conclusion
Driver Architecture

\[ V_{top1} = \frac{2}{3} V_{in} \]

\[ V_{top2} = \frac{1}{3} V_{in} \]

\[ V_{top3} = \frac{1}{3} V_{in} \]

\[ V_{bot1} = \frac{1}{3} V_{in} \]

\[ V_{bot2} = \frac{1}{3} V_{in} \]

\[ V_{bot3} = \frac{1}{3} V_{in} \]
3-Level Gate Signaling Drivers

- No dedicated power rails
- No complex high power stacked drivers
- No level shifters
- Ensures no transistor exceeds the rating

Inverter-based driver
Driver Architecture

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Driver Architecture

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New Level-Shifter Topology (0: \(V_{in}/3 \rightarrow 2V_{in}/3:V_{in}\))

- All digital
- No caps
- Body biasing for fast transition & low power

This topology ensures no transistor exceeds \(V_{in}/3\)

\[
\begin{align*}
&\frac{1}{3}V_{in} & \frac{2}{3}V_{in} \\
\text{in} & \frac{1}{3}V_{in} & \frac{2}{3}V_{in} \\
\bar{\text{in}} & \frac{1}{3}V_{in} & \frac{2}{3}V_{in} \\
\text{out} & V_{in} & V_{in} \\
\bar{\text{out}} & \frac{2}{3}V_{in} & \frac{2}{3}V_{in} \\
& \frac{1}{3}V_{in} & \frac{1}{3}V_{in}
\end{align*}
\]

\[T_d = 230\text{ps} \& P=1.27\text{nW} \at Freq=1kHz \& Vin=4.2V\]
DCM-Operated Top-Level Architecture

DCM is favorable mode for low power applications

- Inherently stable
- High efficiency
- PFM controlled

Inherently stable
PFM controlled
High efficiency

Level Shifters + Drivers

CCM suffers from poor efficiency at low load
Constant On-Time PFM Control

FSM checks the comparator output only at the end of $\phi_6$

- Not to interrupt the flying cap charge balance
- Reduce $F_{sw}$

$V_{out} > V_{ref}$
$\text{CMP} = 1$

FSM triggers $\phi_{FW}$

$V_{out} < V_{ref}$
$\text{CMP} = 0$

FSM triggers new switching cycle
Outline

- Prior Work
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Chip Microphotograph

① Flying caps \((C_{f1}=C_{f2}=5nF)\) \([0.8084\text{mm}^2]\)
② Inductor \((L=3nH, DCR=200m\Omega)\) \([0.4356\text{mm}^2]\)
③ Power stage & drivers \([0.06\text{mm}^2]\)
④ Digital controller \([0.000225\text{mm}^2]\)

Implemented in 10-ML 28nm FDSOI
Total Area = 1.5mm²
Efficiency Measurement

\[ V_{in}=3.6V \]

\[ V_{out}=0.6V \]
\[ V_{out}=0.8V \]
\[ V_{out}=1V \]

\[ \eta_{pk}=78\% \ @ V_{out}=1V \]

\[ 10\mu W < P_{out} < 40mW \]

\[ V_{in}=4.2V \]

\[ V_{out}=0.6V \]
\[ V_{out}=0.8V \]
\[ V_{out}=1V \]
\[ V_{out}=1.2V \]

\[ \eta_{pk}=73.5\% \ @ V_{out}=1.2V \]
Efficiency Measurement

**V_{in}=3.6V**

- $V_{out}=1V$: +47.6%
- $V_{out}=0.8V$: +41.5%
- $V_{out}=0.6V$: +38.9%

**V_{in}=4.2V**

- $V_{out}=1V$: +47.7%
- $V_{out}=1.2V$: +45%
- $V_{out}=0.8V$: +44.7%
Load step (10µA → 1mA) demonstrates:

- PFM control
- Negligible droop and output ripple = 12mV
## Comparison with Prior State-of-Art

<table>
<thead>
<tr>
<th></th>
<th>Breussegem, JSSC’11</th>
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<tr>
<td><strong>Technology</strong></td>
<td>90nm</td>
<td>65nm</td>
<td>180nm</td>
<td>130nm</td>
<td>28nm FDSOI</td>
</tr>
<tr>
<td><strong>Li-ion Capability</strong></td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td><strong>Topology</strong></td>
<td>SC</td>
<td>SC</td>
<td>SC</td>
<td>3-Level</td>
<td>4-Level</td>
</tr>
<tr>
<td><strong>L (H) / No of phases</strong></td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>4n / 4 phases</td>
<td>3n / 1 phase</td>
</tr>
<tr>
<td><strong>CR</strong></td>
<td>1/2</td>
<td>1/3, 2/5</td>
<td>117 CRs</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Vin (V)</strong></td>
<td>3-3.9</td>
<td>3-4</td>
<td>3.4-4.3</td>
<td>2.4</td>
<td>2.8 - 4.5</td>
</tr>
<tr>
<td><strong>Vout (V)</strong></td>
<td>1.3@Vin=3</td>
<td>1.42@Vin=3.3</td>
<td>0.45-1.5</td>
<td>0.4-1.4</td>
<td>0.6-1.2</td>
</tr>
<tr>
<td><strong>F_{max} (MHz)</strong></td>
<td>70</td>
<td>300</td>
<td>2.7</td>
<td>200</td>
<td>200</td>
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<tr>
<td><strong>P_{out} (mW)</strong></td>
<td>1*-150</td>
<td>6*-162</td>
<td>0.001*-0.45</td>
<td>120*-1000</td>
<td>0.01-40</td>
</tr>
<tr>
<td><strong>Dynamic Range (P_{max}/P_{min})</strong></td>
<td>150</td>
<td>27</td>
<td>450</td>
<td>8.3</td>
<td>4,000</td>
</tr>
<tr>
<td><strong>Area (mm²)</strong></td>
<td>3.6*</td>
<td>0.64</td>
<td>1.69</td>
<td>5</td>
<td>1.5</td>
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<tr>
<td><strong>Overall peak efficiency @1/CR</strong></td>
<td>77.3%@2.3</td>
<td>74.3%@3.6</td>
<td>72%@2.6</td>
<td>77%@2.2*</td>
<td>78%@3.6</td>
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<td><strong>Maximum improvement over LDO@ (1/CR)_{range}</strong></td>
<td>33.9%* @2.3</td>
<td>35-45%* @3-4</td>
<td>21%-49.5%* @3-7</td>
<td>18-31%* @2-4</td>
<td>34-50.5% @3-7</td>
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**PFM control**

\[ F_{sw-out} \leq 200\text{MHz} \]

\[ 1\text{kHz} \leq F_{sw-in} \leq 67\text{MHz} \]
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- Proposed Hybrid Architecture
- Switching Phases of the Proposed Architecture
- Circuit Details
- Measurement Results
- Conclusion
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- This work demonstrated that integrating a DC-DC converter compatible with Li-ion battery voltage (2.8-4.2V), using low-voltage transistors (1.5V) in scaled CMOS is feasible.
- A modified 4-level topology was proposed to reduce the cap area by 4x.
- The proposed architecture is DCM-operated to achieve high efficiency at a low load range appropriate for IoT applications (10µW-40mW).
- The proposed converter achieved a peak efficiency of 78% and 34%-50.5% efficiency improvement over an ideal LDO.

The authors thank ST Microelectronics for chip fabrication.