A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving $0.7W/mm^2$ Power Density and 94% Peak Efficiency

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Motivation

- Consumer electronics are shrinking down while performance demand is increasing:

More power demand in a smaller area without sacrificing battery life

PCB of iPhone Xs Max*

*https://www.techinsights.com/
Motivation

- Tradeoff between efficiency and power density:

![Diagram showing tradeoff between efficiency and power density.](image-url)

- High $\eta$ (High efficiency) and Low PD
- Low $\eta$ (Low efficiency) and High PD

New topologies & better packaging

Design points
Conventional Buck Converter

**Survey of compact commercial inductors**

- Bulky inductor (for low DCR)

- **Challenge:** Shrinking inductor increases losses

**PMIC only:**
- PD > 1W/mm²

**Total footprint (including inductor):**
- PD << 1W/mm²

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Building Up The PS3B Converter

- Starting from a conventional buck converter:

\[ V_{IN} \approx V_{OUT} \]

\[ I_{OUT} > I_{IN} \]

Inductors are placed at the high-current side of the converter
Building Up The PS3B Converter

- Moving the inductor to the input-side:

**Passive-stacked 3rd order buck (PS3B) converter**

**Inductors are placed at the low-current side of the converter**

- Split into two half-sized inductors and stack at input
- The input capacitor is now flying
- All passives are stacked at input

High Voltage
Low Current

- Switches (Small $R_{ON}$)

Low Voltage
High Current

- Small Inductor (Large DCR)
Motivation

PS3B Topology
- Basic operation
- Loss-related benefits
- Noise-related benefits
- Structure-related benefits

Converter Implementation

Measurement Results
### Converter Basic Operation

- **Voltage at switching nodes:**

  - $V_{X1} = V_{OUT} - V_{IN}$
  - $V_{X2} = V_{OUT} + V_{IN}$

  What is the relation between $V_{IN}$ and $V_{OUT}$?
Converter Basic Operation

- Inductor volt-second relations:

\[ L_1: (V_{\text{in}} - V_{\text{out}})D + (V_{\text{in}} - V_F - V_{\text{out}})(1-D) = 0 \]

\[ L_2: (V_{\text{out}} - V_F)D + V_{\text{out}}(1-D) = 0 \]

\[ V_F = V_{\text{in}} \quad \text{V}_{\text{out}} = D V_{\text{in}} \]

Relation between \( V_{\text{in}} \) and \( V_{\text{out}} \) is the same as a buck converter

But achieved through 3 passive elements

Hence it is a 3\textsuperscript{rd} order buck*

Flying capacitor stability:

\[ Q_{IN} = DI_{LOAD} (1-D)T_{SW} \]

\[ Q_{OUT} = (1-D)I_{LOAD} DT_{SW} \]

\[ C_F \text{ is stable at } V_{IN} \]
Outline

- Motivation

- PS3B Topology
  - Basic operation
  - Loss-related benefits
  - Noise-related benefits
  - Structure-related benefits

- Converter Implementation

- Measurement Results
Loss-Related Benefits

Conventional Buck

\[ P_{LOSS,DCR,BUCK} = I_{RMS}^2 \times DCR \approx I_L^2 \times DCR \]

- Conduction Loss [mW]
- Duty Cycle
- \( I_{LOAD} = 2A \)
- \( F_{SW} = 6MHz \)
- \( R_{SW} = 8m\Omega \)

Conv. Buck: 1 X 2.56mm³, DCR = 24mΩ (1x)
8.2: A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving 0.7W/mm² Power Density and 94% Peak Efficiency

\[
P_{\text{LOSS,DCR,BUCK}} = I_{\text{RMS}}^2 \times \text{DCR} \approx I_L^2 \times \text{DCR}
\]

\[
P_{\text{LOSS,DCR,PS3B}} = I_{\text{RMS}}^2 \times \text{DCR} \approx n \times I_L^2 \times \text{DCR}
\]

\[n = 1 - 2D + 2D^2 \rightarrow (0.5 < n < 1)\]

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Noise-Related Benefits

Conventional Buck

- Full swing $I_L$
- Full swing $I_2$
- Pulsated $I_1$
- Pulsated $I_2$

PS3B Converter

- Continuous $I_1$
- Continuous $I_2$

Noise and EMI at the input

Additional input filtering may be required

Substantially reduced noise and EMI at input

No need for input capacitor OR inductor

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Structure-Related Benefits

The power stage and the load are separated by the output filter

Direct connection between the power stage and the load

Stacked passives minimize routing overhead

Load can be integrated with power stage on a single die
Motivation

PS3B Topology
- Basic operation
- Loss-related benefits
- Noise-related benefits
- Structure-related benefits

Converter Implementation

Measurement Results
Implementing Power MOSFETs

Non-standard voltage levels are required to drive the power MOSFETs.

These voltage levels are available at the two switching nodes $V_{X1}$ and $V_{X2}$.
MOSFET Drivers Using Bootstrapping Capacitors

- \( C_{\text{boot1}} \) stores the \((V_{\text{OUT}} + V_{\text{IN}})\) level and is used to drive \( M_1 \)
- \( C_{\text{boot2}} \) stores the \((V_{\text{OUT}} - V_{\text{IN}})\) level and is used to drive \( M_2 \)
- Power MOSFETs are driven from the internal nodes
**Converter Full Schematic**

**Bottom plate of** $C_{boot1}$ **and top plate of** $C_{boot2}$ **are connected to** $V_{OUT}$ **instead of ground**

**Both** $C_{boot1}$ **and** $C_{boot2}$ **block** $V_{IN}$ **only**

**Up to 4x saving in capacitor implementation area**

**$C_{F,on-chip}$ is used to mitigate potential ringing on driver lines**

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**8.2: A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter**

Achieving 0.7W/mm² Power Density and 94% Peak Efficiency
All the drivers are powered from the internal nodes of the converter.

Four level-shifted control signals are generated from a single PWM signal.
No need for external supplies for level shifters.
PMIC Implementation

Standard devices

The chip bulk is biased to $V_{OUT}^*$

No need for the ground signal inside the PMIC.

*Not strictly required, the chip bulk can be biased to ground but with more DNW devices.

DNW devices

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PMIC Implementation

Switching losses:
- Parasitic capacitance of both power MOSFETs experience same $\Delta V$ as a buck converter.
- PS3B and conventional buck converter have same switching losses.

The current ripple at the output is doubled:
- Need to use larger output capacitor.
- In this design, 0.47 $\mu$F was sufficient to get output ripples <30mV.
Total footprint: 5mm² including all the passives and the routing

Passives stacked at the input allows for saving in the routing area
Outline

- Motivation

- PS3B Topology
  - Basic operation
  - Loss-related benefits
  - Noise-related benefits
  - Structure-related benefits

- Converter Implementation

- Measurement Results
A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter
Achieving 0.7W/mm² Power Density and 94% Peak Efficiency

**Chip Summary**

<table>
<thead>
<tr>
<th>Process</th>
<th>0.18μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMIC Area</td>
<td>1.85mm²</td>
</tr>
<tr>
<td>VIN</td>
<td>1.8V</td>
</tr>
<tr>
<td>VOUT</td>
<td>0.5 – 1.5V</td>
</tr>
<tr>
<td>ILOAD</td>
<td>0.1 - 2.5A</td>
</tr>
<tr>
<td>FSW</td>
<td>6.5MHz</td>
</tr>
</tbody>
</table>
Switching nodes

\[
\begin{align*}
V_{IN} &= 1.8V, \\
V_{OUT} &= 1V \\
V_{X1} &= 1V \rightarrow 2.8V \\
V_{X2} &= -0.8V \rightarrow 1V
\end{align*}
\]

Correct levels for switching nodes

Measured Waveforms

Continuous input current

Input current & output ripples

Transient response
A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter
Achieving 0.7W/mm² Power Density and 94% Peak Efficiency

### Measured Efficiency

- $\eta_{\text{peak}} = 94\%$ @ PD of 0.18W/mm²
- Max. PD of 0.7W/mm² @ 86.6%
8.2: A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter
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*Only switched-capacitor or resonant converters are shown with a high number of conversion ratios to mimic a continuous conversion ratio for DVFS-enabled voltage regulation.
# Table of Comparisons

<table>
<thead>
<tr>
<th>Topology</th>
<th>Kim JSSC’15</th>
<th>Lee ISSCC’17</th>
<th>Liu ISSCC’17</th>
<th>Jia JSSC’18</th>
<th>Jiang ISSCC’18</th>
<th>TI TPS8268150</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>Buck 65nm</td>
<td>Buck 350nm</td>
<td>Hybrid 65nm</td>
<td>Buck 65nm</td>
<td>65nm 65nm</td>
<td>NR 180nm</td>
<td>Hybrid (PS3B)</td>
</tr>
<tr>
<td>Input Voltage [V]</td>
<td>1.8 3.3</td>
<td>3.0 – 4.5</td>
<td>1.1 0.22 – 2.4</td>
<td>2.3 - 5.5</td>
<td>0.5 – 1.5</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>Output Voltage [V]</td>
<td>0.6 – 1.5</td>
<td>0.3 – 2.5</td>
<td>0.3 – 1.0</td>
<td>0.3 – 0.86</td>
<td>0.85 – 1.2</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>I_{LOAD} (MAX) [A]</td>
<td>0.6 6</td>
<td>1.53 0.04</td>
<td>0.08 1.6</td>
<td>2.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current</td>
<td>Pulsated</td>
<td>Pulsated</td>
<td>Pulsated</td>
<td>Pulsated</td>
<td>Pulsated</td>
<td>Continuous</td>
<td></td>
</tr>
<tr>
<td>PMIC Area [mm²]</td>
<td>5 1.88</td>
<td>4.05 0.13</td>
<td>2.42 6.67</td>
<td>1.85</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Footprint [mm²]</td>
<td>5 NR 6**</td>
<td>0.13 2.42</td>
<td>6.67 5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Efficiency (PE)</td>
<td>95.5% 88.1%</td>
<td>94.2% 73%</td>
<td>84.1% 88%***</td>
<td>94%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Density @ PE* [W/mm²]</td>
<td>0.03*** NR****</td>
<td>0.04** NR</td>
<td>0.013 0.045***</td>
<td>0.18 (0.25**)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Power Density (PPD)* [W/mm²]</td>
<td>0.17 NR****</td>
<td>0.24 0.27 0.34***</td>
<td>0.36***</td>
<td>0.7 (1.0**)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency @ PPD</td>
<td>88% NR****</td>
<td>88.3% NR</td>
<td>74%*** 74%***</td>
<td>86.6%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Unless otherwise specified, power densities are computed with respect to the total converter footprint including the passives and routing
** Computed by summing the area of the passive component footprints
*** Estimated from measurement results
**** The area of the passives are not reported
Summary

- **A 3rd order buck is introduced:**
  - Reduced conduction loss.
  - Continuous input current.
  - Small passives stacked at the input.

- Achieves a high power density amongst prior-art converters that operate @ >85% efficiency with continuous conversion ratios across SoC-compatible voltage ranges.

- Achieves comparable peak efficiency (94%) @ >4x higher power density than prior-art.

- Has a unique feature of continuous input current, which would help minimize the area needed for on-board filtering.

Acknowledgement: pSemi Corporation
Backup slides
Converter Full Schematic

Bottom plate of $C_{boot1}$ and top plate of $C_{boot2}$ are connected to $V_{OUT}$ instead of ground.

Both $C_{boot1}$ and $C_{boot2}$ block a $V_{IN}$ only increasing their effective capacitance and reducing their required rating.

Saving in capacitor implementation area of up to 4x.

$C_{F,on-chip}$ is used to mitigate potential ringing on driver lines.