Enabling Sub-nW RF Circuits through Subthreshold Leakage Management

Patrick P. Mercier*, Saurav Bandropadhyay†, Anantha P. Chandrakasan‡
* University of California San Diego, La Jolla, CA, USA
† Texas Instruments, Dallas, TX, USA
‡ Massachusetts Institute of Technology, Cambridge, MA, USA
Email: pmercier@ucsd.edu

***Abstract* — This paper presents subthreshold leakage management techniques to enable the design of a 2.4 GHz RF transmitter with ultra-low average power. Careful device size optimizations and judicious use of power gating devices shows that leakage power of the radio can be reduced by upwards of 4000X. When operating at a duty-cycled average data rate of 1 b/s, the implemented transmitter consumes 78 pW.**

I. Introduction

In today's "Internet of Things" era, there are a large number of emerging applications such as wearable monitors, implanted sensors, and smart appliances that require wireless connectivity in ultra-miniature form factors. Unfortunately, most commercial and research-based radios require > 100 µW of power during continuous operation [1]–[3], which typically dominates system power budgets and necessitates large batteries or energy harvesters for long-term use. To reduce overall system size, we exploit the fact that many emerging applications have low average data rate requirements, permitting the duty-cycling of radios between high-power active mode and low-power standby mode.

The challenge here is that RF circuits naturally require fast transistors to operate at RF frequencies; however, such transistors generally have low threshold voltages and minimal lengths, and as a result, generally have substantial subthreshold leakage currents. In this paper, we will explore sizing and gating techniques to minimize the leakage power of both peripheral and RF circuits in order to reduce the *average* power consumption during aggressively duty-cycled operation. We will validate such techniques through the design of a sub-nW RF transmitter, whose architecture is shown in Figure 1 [4].

II. Sizing for Leakage & Performance

A. Trade-offs

It is well-known that high-V_t devices have larger I_{on} to I_{off} ratios than low-V_t devices sized to deliver the same amount of on-current. Thus, a design using high-V_t devices will generally offer the lowest amount of total subthreshold leakage power. However, choosing a high-V_t device over a low-V_t device has consequences in regards to device size, and as a result, parasitic capacitance. For example, parasitic capacitance can increase by 3-10X between low-V_t and high-V_t devices in 0.18 µm CMOS.

B. Low-Frequency Circuits

For sub-systems that have low frequency requirements such as digital control, watchdog timers, and other peripherals circuits that must operate continuously, operational speed is typically not critical and exclusive use of high-V_t devices is often appropriate. To minimize leakage, the standard subthreshold current equation, $I_{DS} = I_{D0}(W/L)\, e^{V_{GS}/n\phi_t}$, suggests employing narrow-*W*, long-*L* transistors. However, many sub-micron technologies (including the chosen 0.18 µm technology) employ the use of shallow trench isolation (STI) to isolate adjacent transistor leakage effects. As the transistor width gets narrower, the electric field at the edge of the trench becomes enhanced, creating a slightly stronger inversion layer, which ultimately causes a drop in threshold voltage. This phenomenon, termed the inverse narrow width effect (or the reverse short channel effect), causes device leakage to be higher for very short width devices [5]. This effect is illustrated in Figure 1 for representative high-V_t NMOS and PMOS devices, where up to 50% leakage reduction can be achieved simply through optimized NMOS sizing.

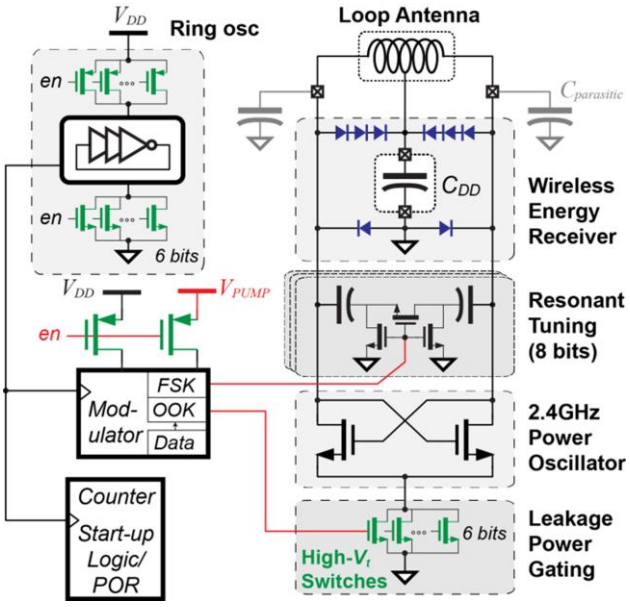

Figure 1. Architecture of the example sub-nW transmitter.

C. High-Frequency Circuits

For sub-systems that have moderate-to-high frequency requirements and that either must operate continuously, or do not have the voltage headroom for power gating (typically encountered in ultra-low voltage designs), then study of sizing-leakage trade-offs are essential to optimizing system performance. For minimum leakage, the standard subthreshold equation predicts that the longest channel length possible is

The authors acknowledge support from the C2S2 Focus Center and the Interconnect Focus Center, two of six research centers funded under the Focus Center Research Program (FCRP), a Semiconductor Research Corporation entity.

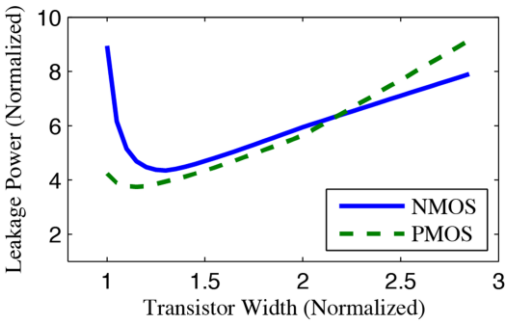

Figure 2. Leakage power minimization through sizing.

optimal. However, this is not necessarily the best choice in practice. Figure 3 shows simulation results of the maximum operational frequency of high-V_t NMOS and PMOS devices in a FO4 configuration for various transistor lengths. Here, it can be seen that a > 2X leakage reduction is achieved by increasing the device length beyond the minimum. However, further increases to device length bring very incremental improvements in leakage power, especially in the NMOS device, at the cost of significant frequency (and CV^2 energy) degradation. Thus, it generally beneficial to operate with device lengths just beyond minimum size as a balance between low-leakage and moderate performance. Similar behavior is observed for low-V_t devices in this process.

III. Power Gating

While sizing optimizations can reduce subthreshold leakage power by 2-3X, power gating can have a far more substantial effect. In fact, so long as the application in question is conducive to duty-cycling, and that there is sufficient voltage headroom, power gating can permit the use of high-performance, low-V_t devices in the critical path with minimal leakage penalty. For example, the cross-coupled power oscillator transistors in Figure 1 are gated with high-V_t footer switches by a higher-than-V_{DD} supply, V_{PUMP}, in order to increase their I_{on} to I_{off} ratios to enable sub-100 pW leakage power while permitting greater than 100 µW active-mode power. Such gating saves upwards of 300X in leakage power over using low-V_t footer devices.

When performance is not as critical, power gating can have an even more substantial effect on the overall circuit leakage. For example, the modulator block in Figure 1 has the vast majority of its logic gates connected to a small number of power gating devices; thus, most of the leakage in the block is set by the small number of header switches. By driving the gates of V_{DD} -supplied PMOS gating transistors from the V_{PUMP} supply, they are able to enter the super-cut-off regime, further reducing leakage power. Altogether, power gating results in up to 4000X and 20X reductions in leakage power from the V_{DD} and V_{PUMP} supplies, respectively.

IV. Example: Ultra-Low-Leakage Transmitter

A 2.4 GHz transmitter was designed using the sizing and power gating techniques described above. The design uses high-V_t devices with optimized sizes nearly exclusively for ultra-low leakage, with three primary exceptions. The cross-coupled RF transistors use low-V_t devices in order to reduce parasitic capacitance on sensitive output RF nodes by 10X for equivalent drive current. Since the resonant tuning DAC switches do not consume static power, they also employ low-V_t devices to maximize linearity and minimize parasitics. Finally, the ring oscillator inverter transistors employ low-V_t devices to save upwards of 10X in CV^2 energy per cycle.

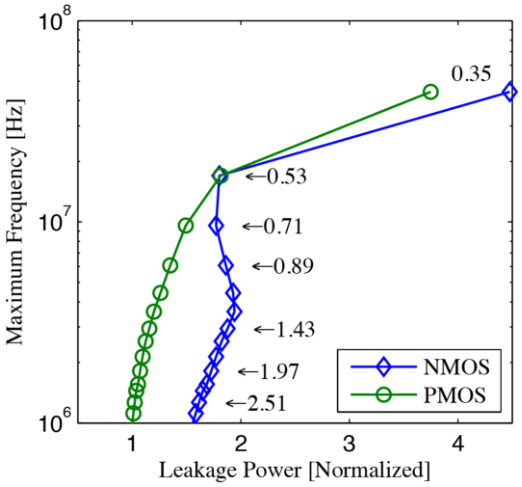

Figure 3. Frequency-leakage sizing trade-off for various sizes of NMOS and PMOS transistor lengths (in µm) with optimized widths for minimum leakage.

Fabricated in a 0.18 µm process, the transmitter consumes a standby power of 39.7 pW at 0.8V. In active mode at an instantaneous data rate of 5 Mb/s, the transmitter consumes 191 µW using OOK modulation. When duty-cycled down to an average data rate of 1 b/s, the transmitter consumes an average of 78 pW. To demonstrate the application-oriented benefit of such a low power radio, the transmitter was integrated with an energy harvester and sensor that demonstrated energy extraction from the biologic battery located in the inner-ear of mammals; the entire system power consumption was approximately 1 nW [6].

V. Conclusion

Sizing optimizations and power gating techniques are both useful tools to enabling subthreshold leakage powers below the nanowatt regime. In this paper we have demonstrated that combining these techniques together with a low-complexity transmitter architecture that employs aggressive duty-cycling can enable a sub-nW wireless transmitter.

References

[1] A.C.W. Wong et al., "A 1 V Wireless Transceiver for an Ultra-Low-Power SoC for Biotelemetry Applications," *IEEE JSSC*, Jul. 2008.

[2] A. Paidimarri et al., "A 2.4 GHz Multi-Channel FBAR-based Transmitter With an Integrated Pulse-Shaping Power Amplifier," *IEEE JSSC*, Apr. 2013.

[3] G. Chen et al., "A cubic-millimeter energy-autonomous wireless intraocular pressure monitor," in *IEEE ISSCC*, 2011, pp. 3010-312.

[4] P.P. Mercier et al., "A 78 pW 1 b/s 2.4 GHz Radio Transmitter for Near-Zero-Power Sensing Applications," in *IEEE ESSCIRC*, 2013.

[5] J.A. Mandelman et al., "Anomalous narrow channel effect in trench-isolated buried-channel p-MOSFET's," IEEE Elec. Dev. Let., 1994.

[6] P.P. Mercier et al., "Energy extraction from the biologic battery in the inner ear," Nature Biotechnology, Dec., 2012.