A Footprint-Constrained Efficiency Roadmap for on-Chip Switched-Capacitor DC-DC Converters

Loai G. Salem & Patrick P. Mercier
University of California, San Diego
Voltage domain challenges in modern SoCs

Example: IBM POWER8

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Challenge: powering 48 independent dynamic voltage and frequency scaling (DVFS) domains
Powering multiple domains

- **Solution 1: inductive converters**
  - **PROS:**
    - High efficiency
    - Large Vin-Vout range possible
  - **CONS:**
    - Inductors are large & do not scale

- **Solution 2: linear regulators**
  - **PROS:**
    - Very small, can fully integrated into SoC
    - Stable, low-noise
  - **CONS:**
    - Efficiency < Vout/Vin; can be very small at large voltage conversion ratios

Source: Sunlord Inc.
Switched-capacitor DC-DC converter: inherent size advantage

• Solution 3: switched-capacitor converters

• PROS:
  • Higher inherent power and energy density than inductors
  • Easily integrated on-chip (e.g., MIM, MOSCAP, DT, etc.)
  • Can leverage existing on-chip decoupling

• CONS:
  • Prior-art has limited output voltage range (limited by discrete conversion ratios)
Solving the output voltage problem via recursive switched capacitor topologies

4-bit RSC

Efficiency [%]

Output Voltage [V]

[8:1, 16:3, 4:1, 3:1, 2:1, 3:2, 4:3, 16:15]

[Salem & Mercier, ISSCC, CICC, JSSC 2014]
Switched Capacitor power density

Power density and efficiency are improving. How much do we need moving forward?

Requires inductors or expensive process options

Source: ISSCC Tech. Trends
Using the *International Technology Roadmap for Semiconductors (ITRS)* as a guideline

This work: focus on consumer-portable SoCs (SoC-CP*)

* Using 2011 numbers, since the 2013 SoC-CP chapter is not currently available online
ITRS canonical cell area

Define $F = \text{Metal 1 half-pitch}$

$$U_{\text{logic}} = 3P_{\text{poly}} \times 8P_{M2} = 180F^2$$

(calibrated $\Rightarrow 175F^2$)

$$U_{\text{SRAM}} = 2P_{\text{poly}} \times 5P_{M1} = 60F^2$$
Computing cell area and power density

- **ITRS**: logic and memory area can be represented by canonical cells (NAND2, SRAM) with overhead factors: $O_{logic} = 2.0$, $O_{SRAM} = 1.6$

**Logic**

$$D_{tr,logic} = \frac{4}{O_{logic}U_{logic}}$$

Transistor density

$$D_{cap,logic} = D_{tr,logic}C_g W_{logic} + D_{l,eff} C_w$$

Trans. unit cap. Wiring cap.

$$P_{dynamic,logic} = \alpha_{logic}\left(\beta + \frac{1}{3}(1 - \beta)\right) D_{cap,logic} f_c V_{DD}^2$$

Not all nodes on critical path – lower activity

**SRAM**

$$D_{tr,SRAM} = \frac{6}{O_{SRAM}U_{SRAM}}$$

Transistor density

$$P_{dynamic,SRAM} = \alpha_{SRAM}D_{tr,SRAM} 2C_g W_{SRAM} f_c V_{DD}^2$$

Cap. per SRAM trans.

**P_{static}: Logic & SRAM**

$$P_{static} = \frac{1}{2} D_{tr} I_{off} V_{DD}$$

Half of all branches leak

Not all nodes on critical path – lower activity
Putting the model together

• To accommodate low-power design techniques such as DVFS, power gating, body biasing, etc., ITRS includes a power improvement factor, $\gamma$

$$P_{\text{logic, total}} = \frac{P_{\text{dyn, logic}}}{\gamma_{\text{dyn}}} + \frac{P_{\text{static, logic}}}{\gamma_{\text{static}}}$$

$$P_{\text{SRAM, total}} = \frac{P_{\text{dyn, SRAM}}}{\gamma_{\text{dyn, SRAM}}} + \frac{P_{\text{static, SRAM}}}{\gamma_{\text{static, SRAM}}}$$

$$P_{\text{chip, total}} = \frac{S_{\text{logic}}P_{\text{logic, total}} + S_{\text{SRAM}}P_{\text{SRAM, total}}}{S_{\text{logic}} + S_{\text{SRAM}}}$$

Total area:

$$O_{\text{logic}}U_{\text{logic}}N_{\text{gates}}$$

$$O_{\text{SRAM}}U_{\text{SRAM}}N_{\text{bits}}$$

• $N_{\text{gates}}$ and $N_{\text{bits}}$ found under ITRS System Drivers chapter
• Assume 250kGate / 1Mbit ratio between logic and memory
Model results

- Input to model from ITRS process integration, devices, and structures (PIDS) chapter

Developed model matches ITRS results to within 15%.

Importantly, breaks out power density of logic and SRAM
Exploiting decoupling capacitance for integrated SC conversion

- All DC-DC converters, including integrated LDOs, use decoupling capacitance.

- Recent work is exploiting this for SC conversion without additional area overhead.

- Optimal amount of decoupling to suppress noise [11]:
  \[ C_{\text{decap}} = \frac{I}{2nf_cV_{DD}} \]  
  \[ \text{Tolerated fractional supply noise} \]

- Assuming \( C_{\text{decap}} \) is included in \( O_{\text{logic}}, O_{\text{SRAM}} \), decap density can be found as:
  \[ D_{\text{decap,logic|SRAM}} = \frac{P_{\text{total,logic|SRAM}}C_{\text{decap}}}{V_{DD}I} = \frac{P_{\text{total,logic|SRAM}}}{2nf_cV_{DD}^2} \]

Scaling decoupling capacitor requirements

For 10% supply variation, decoupling needs stay ~constant at 0.5nF/mm²
A footprint-constrained SC roadmap: efficiency

• 2:1 SC losses can be summarized by: [4]

\[
\frac{P_{\text{loss}}}{P_L} = 3^3 \sqrt{2 \frac{I_L}{D_{\text{cap}}} \frac{R_{\text{on}} C_g}{V_{DD}}}
\]

Current density

Switch resistance and capacitance

Capacitance density

• Recall that \( \frac{I_L}{D_{\text{cap}}} = 2nf_c V_{DD} \), and thus:

\[
\tau = R_{\text{on}} C_g \text{ (intrinsic transistor delay)}
\]

Losses of SC converter using on-chip decoupling capacitance

Depends on frequency-transistor delay product

A footprint-constrained SC roadmap: results

Constraining ourselves to only using area required for decoupling in future nodes, achievable power density increases with scaling, and efficiency is > 80%.
Conclusions

- Switched capacitor DC-DC converters offer both high-efficiency and small size
  - Output voltage ranges are getting better
- Recent work has shown ultra-high power density is achievable, yet requires:
  - Inductors
  - Expensive process options
- This work presented a model describing the achievable efficiency and power density of SC converters with no area penalty by using on-chip decoupling
- 0.5W/mm$^2$ is sufficient in current-generation technologies, 1-2W/mm$^2$ easily achievable in future technologies using only MOS capacitors
- Deep-trench or resonant converters may not be necessary to meet the demands of current and future SoC-CP applications