An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range

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Parallelism, The Way For Higher Processing

• Higher-frequency exceeds thermal limits

High performance & low power:
- Parallel processing (multi-core)

No. of processing engines exponentially increases to meet customer expectations

Per-module voltage scaling for adapting power with processing load

Fully-integrated DC-DC Converters are required

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4.6: An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range

T5 SPARC, 16 Core, ISSCC’13
Outline

- On-Die DC-DC Converters
- Recursive SC Topology
- All Digital Binary Search Control
- Measurement Results
- Conclusions
Linear Voltage Regulator

• A resistive divider

<table>
<thead>
<tr>
<th>Compact</th>
<th>Very lossy when $V_{DD}$ goes far below $V_{IN}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>No switching noise</td>
<td></td>
</tr>
<tr>
<td>Fast</td>
<td></td>
</tr>
</tbody>
</table>

$V_{drop} = \frac{V^2}{R_{pass}}$

$\eta = \frac{V_{DD}}{V_{IN}}$

Error Amplifier

$V_{ref}$

$V_{IN}$

$V_{DD}$

$R_{pass}$

Load: $R_L$

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Switched Capacitor DC-DC Converters

• How to convert input DC voltage?

Switched Capacitor
Switched Capacitor DC-DC Converters

• How to convert input DC voltage?

Switched Capacitor

\[
V_{IN} \quad 2V_{IN} \\
\Phi_2 \\
\Phi_1 \quad C
\]

Voltage doubler
fixed 1:2 conversion

\[
V_{DD} = 2V_{IN}
\]

\[
C \quad + \quad V_{in} \\
- \\
V_{IN}
\]

\[
V_{IN} \quad C \quad - \\
\Phi_1
\]

\[
\Phi_2
\]
Switched Capacitor DC-DC Converters

• How to convert input DC voltage?

Swap $V_{IN}$ and $R_L$ for $V_{IN}/2$ instead of a $2V_{IN}$

$V_{out} = 2V_{IN}$

$V_{out} = V_{IN}/2$
Why $\eta \neq 100\%$?

\[ V_{out} = V_{IN}/2 \]

Large decoupling cap $C_{out}$
SC Loss

- Why SC $\eta \neq 100\%$?

\[ q_{out} = 2q \]
\[ V_{IN} q = V_{IN}/2 \]
\[ 2q \]
\[ E_{in} = E_{out} \]

Charge-discharge diagram with equations:

\[ V_{IN} \]
\[ C \]
\[ q \]
\[ V_{out} = V_{IN}/2 \]
\[ C_{out} \]
\[ R_L \]

Charging and discharging processes.
SC Loss

- Why SC $\eta \neq 100\%$?

$E_{loss} = C\Delta V^2$

No $R_{on}$ dependence

$\frac{1}{2} C \Delta V^2$

$V_{out} = \frac{V_{IN}}{2}$

$\Delta V \uparrow \Rightarrow \Delta V \downarrow$

$f_{sw} \uparrow \Rightarrow \Delta V \downarrow$

Charging

Discharging
• Loss can be modeled by $R_{out}$

This is how to provide continuous conversion: change $R_{out}$ like an LDO

$V_{out}$

$V_{IN}/2$

$R_{out}$

$2R_{on}$

$\Delta V$ decreases

$f_{SW}$

$f_{SW}$

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7 of 35
Series-Parallel SC Efficiency

Efficiency vs. $V_{out}$ at $V_{in} = 2.5V$

Requires more ratios

2:1 SC
3:2 SC
3:1 SC

Efficiency [%]

Output Voltage [V]

Ideal LDO

2:1
3-ratio

$V_{out}$ at $V_{in} = 2.5V$

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Problem: Given certain C, re-use that to produce different ratios

- No. Of caps and switches increases exponentially
- Each ratio requires a unique arrangement, which is difficult to re-use among other ratios

Higher no. of ratios requires a **Modular topology**
SC 4:1 Series-Parallel

• Conventional 4:1

\[ V_{out} = \frac{V_{IN}}{4} \]

<table>
<thead>
<tr>
<th>Cap no.</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW no.</td>
<td>10</td>
</tr>
</tbody>
</table>

\[ V_{IN} = 4V_{out} \]

\[ + \quad V_{out} \quad + \quad V_{out} \quad - \quad V_{out} \quad - \quad V_{out} \]

\[ + \quad V_{out} \quad + \quad V_{out} \quad - \quad V_{out} \quad - \quad V_{out} \]

\[ + \quad V_{out} \quad + \quad V_{out} \quad - \quad V_{out} \quad - \quad V_{out} \]

C \quad C \quad C \quad C

C \quad C

C \quad C

\[ V_{out} \]

\[ V_{out} \]

\[ R_L \]

\[ C_{out} \]

Parallel

Series

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Proposed Modular Switched-Capacitor Topology

- **Ratio = 1/4**
- Connect a second 2:1 cell \((C_2)\) between cell \((C_1)\) output & GND

\[
V_{out} = V_{IN}/4
\]

<table>
<thead>
<tr>
<th>SP</th>
<th>New 1/4</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/4</td>
<td></td>
</tr>
</tbody>
</table>

| Cap no. | 3 | 2 |
| SW no.  | 10 | 8 |
Proposed Modular Switched-Capacitor Topology

- Ratio = 3/4
- Connect the second 2:1 cell \((C_2)\) between \(V_{\text{IN}}\) & cell \((C_1)\) output

\[
V_{\text{out}} = \frac{(V_{\text{in}} + V_{\text{in}}/2)}{2} = \frac{3V_{\text{IN}}}{4}
\]

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</table>
SC Ratio Reconfiguration

- 1/4, 3/4 are realized, how to get 1/2

**Cells Stacked for 3/4**

\[ V_{\text{out}} = \frac{3V_{\text{IN}}}{4} \]

**Route \( V_{\text{out}} \) from 1\(^{st}\) cell for 1/2**

\[ V_{\text{out}} = \frac{V_{\text{IN}}}{2} \]

**Cells cascaded for 1/4**

\[ V_{\text{out}} = \frac{V_{\text{IN}}}{4} \]

Wastes the capacitance of the 2\(^{nd}\) cell, lower \( \eta \)
Recursive SC Ratio Reconfiguration

- 1/4, 3/4 are realized, how to get 1/2

**Cells Stacked for 3/4**

\[\text{Cells in parallel for 1/2} \]

\[V_{\text{out}} = 3V_{\text{IN}}/4 \]

**Cells cascaded for 1/4**

\[V_{\text{out}} = V_{\text{IN}}/2 \]

**Recursive Inter-cell Connection:** 100% of the Caps used among all ratios
Recursive Inter-Cell Connection

• How to realize 1/2, the switch detail

\[ V_{IN} \]

\[ V_{out} \]

\[ \phi_1 \cdot \phi_2 \]

\[ C_1 \]

\[ C_2 \]

\[ V_{out} \]

Ratio = 1/2
two cells in parallel
Recursive Inter-Cell Connection

- How to realize 1/4, the switch detail

\[ V_{\text{IN}} \]

\[ V_{\text{out}} \]

\[ V_{\text{out}} \]

\[ S_{R2} \quad S_{R1} \]

\[ S_{R3} \quad S_{R4} \]

\[ C_1 \quad C_2 \]

Ratio Reconfiguration Switches
Recursive Inter-Cell Connection

- How to realize 1/4, the switch detail

\[ V_{IN} \]

\[ S_{R2} \]

\[ S_{R3} \]

\[ V_{out} \]

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ C_1 \]

\[ C_2 \]

\[ \text{Disabled} \]

\[ V_{out} \]

\[ S_{R2} \] & \[ S_{R3} \] work as OUTPUT switches
Recursive Inter-Cell Connection

• How to realize 1/4, the switch detail

$V_{IN}$

$V_{out}$

$S_{R2}$ $S_{R1}$

$S_2$ $S_1$

$S_{R3}$

$C_1$ $C_2$

$S_{R1}$ works as INPUT switch $S1$
Recursive Inter-Cell Connection

- How to realize $1/4$, the switch detail

$$\text{Ratio} = 1/4$$

two cells in cascade

$$V_{out} = \frac{\text{MID}}{2}$$
Recursive Inter-Cell Connection

- How to realize 3/4, the switch detail

\[ V_{IN} \]

\[ S_{R2} \]

\[ S_{R3} S_{R4} \]

\[ V_{out} \]

\[ S4 \]

\( S_{R4} \) works as GND switch S4

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ \Phi_3 \]

\[ \Phi_4 \]

\[ GND \]

\[ \text{Disabled} \]
Recursive Inter-Cell Connection

- How to realize 3/4, the switch detail

\[ V_{out} = \frac{(V_{IN} + \text{MID})}{2} \]

**Ratio** = 3/4

*two cells are stacked*
• Adding a third 2:1 SC cell: \( \text{resolution} = \frac{V_{\text{in}}}{2^3} \)

\[ V_{\text{out}} = \frac{V_{\text{in}}}{8} \]
Realizing 3/8 ratio

\[ V_{out} = \frac{3V_{in}}{8} \]

Move 2\textsuperscript{nd} cell UP
Another way to realize 3/8 ratio

\[ V_{out} = \frac{(V_{in}/2 + V_{in}/4)}{2} = \frac{3V_{in}}{8} \]
Recursive 3-bit SC

• Which one is better to realize 3/8 ratio?

\[ \frac{3V_{\text{IN}}}{8} \]
Recursive 3-bit SC

- Which one is better to realize 3/8 ratio?

**Binary relative sizing**

1st Cell is loaded by extra \( \frac{q}{2} \)

For same \( q \) output, SC is less loaded, thus lower losses

Maximizing \( V_{in} \) & GND connections maximizes \( \eta \)

Higher \( \eta \)

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Recursive 3-bit SC: 1/2 Realization

- Now 1/8, 3/8, 5/8, 7/8 are realized, how to achieve 1/2 using 3 cells?

Recursion:
Connect 3 cells in parallel for 1/2

Cells connected in cascade for \( n_{\text{odd}}/8 \)
Recursive 3-bit SC: 1/4, 3/4 Realization

- Now 1/8, 3/8, 5/8, 7/8, and 1/2 are realized, what about 1/4, 3/4?

\[ \frac{V_{out}}{V_{in}} = \frac{3}{4} \]

Vout = \frac{3V_{in}}{4} \text{ into 2 cells}

Put the 2 slices in cascade & in parallel to the other 2 cells’ cascade

\[ V_{out} = \frac{3V_{in}}{4} \]

\[ V_{out} = \frac{V_{in}}{2} \]
Recursive 4-bit SC

• A 4-bit Recursive SC topology is implemented
  • Balance between complexity and flat $\eta$

Realizing 15-ratio, of high $\eta$ by:
  ➢ Recursive inter-cell connection for 100% cap utilization
  ➢ Maximizing $V_{in}$ & GND connections
  ➢ Binary relative sizing
For same silicon area: widest operating range, highest average efficiency
Typical Multi-Mode SC Control

• Compare $V_{\text{ref}}$ (desired output) with levels from a resistor string to find desired ratio
• Challenge of large number of ratios

For 8-bit resolution~256 accurate resistors and comparators are needed
• Ratios’ threshold levels mismatch due to SC

\[ R_{out} \]

\[ f_{sw} \]

\[ V_{out} \]

\[ n/mV_{IN} \]

\[ R_{out1} \]

\[ R_{out2} \]

\[ R_{out3} \]

\[ R_2 \]

\[ R_1 \]

\[ R_0 \]

\[ R_{2^N-1} \]

\[ R_{2^N-2} \]

\[ R_{out} \text{ changes from one ratio to another} \]
All-Digital Binary Search Control

• Solution: Ratios’ threshold levels are produced by the SC itself

Switching at highest $f_{sw}$, $R_{out}$ is min

SC outputs the max $V_{out}$ for certain $n/m$ RATIO
All-Digital Binary Search Control

- Binary Search Algorithm:

  - **Strobe Reset:** \( R = \frac{1}{2} \)

  - **Apply Ratio:** \( V_{out} = R \times V_{in} \)

  - **Depth \( \leq 4 \)**

  - **End**

  - **No** \( V_{out} > V_{ref} \)

  - **Yes**

  - **Go to higher binary ratio** \( R_n = \frac{1+R_{n-1}}{2} \)

  - **Go to lower binary ratio** \( R_n = \frac{R_{n-1}}{2} \)

- **Max resolution** \( V_{in}/2^2 \)

  - **Control logic**

  - **SC**

  - **V_{in}**

  - **V_{ref}**

  - **V_{out}**

- **No resistor string**
- 1 comparator & simple gates
- No \( R_{out} \) mismatch

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• 8 µs response time

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**Measured Controller Transient Response**

- **8 µs response time**

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Fully Integrated Recursive 4-bit SC Prototype

- 8 2:1 cells are used to enable recursion
- Cells are binary weighted for optimal relative sizing

0.25\textmu m 2.5V bulk CMOS
MIM \sim 0.9 fF/\textmu m^2
For same silicon area: widest operating range, highest average efficiency

0.25\(\mu\)m: Cap = 3nF, \(V_{in} = 2.5\), \(I_L = 2\)mA

• This work (measured)
• \(\eta_{peak} = 85\%\)

- Measurements within 1\% of the Model

predicted \(\eta\) by model

\(\frac{4}{3} : \frac{2}{1}\)

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0.25μm: C = 3nF, V_{in} = 2.5, \textbf{Ratio} = 1/2

\begin{align*}
\text{Switching losses scale with lower power levels}
\end{align*}
• Tracking an input stair control voltage

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Conclusions

• A new Modular SC topology comprising individual 2:1 SC
• High $\eta$ through:
  • *Recursive interconnection* achieving 100% cap utilization
  • *Maximizing $V_{in}$ & GND connections* for minimum overhead charge through the SC
  • *Optimal resource allocation* $(C,G)$ through *BINARY* relative sizing

*Highest average $\eta$ & widest operating range amongst other SC topologies for same silicon area*