A 78 pW 1 b/s 2.4 GHz Radio Transmitter for Near-Zero-Power Sensing Applications

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***Abstract*—This paper presents an ultra-low-standby-power radio transmitter that was designed for applications with extreme energy storage and/or energy harvesting constraints. By utilizing aggressive power gating techniques within a low-complexity architecture featuring only a single RF stage, the transmitter achieved a standby power consumption of 39.7 pW. The architecture employed a direct-RF power oscillator that featured an on-board loop antenna that functioned as both the resonant and radiative element. Supporting both OOK and FSK modulations, the transmitter consumed 38 pJ/bit at an instantaneous data rate of 5 Mb/s. After duty-cycling down to an average data rate of 1 b/s, the transmitter consumed an average power of 78 pW.**

***Index Terms*—body-sensor networks, CMOS, low power electronics, narrowband, power amplifiers, radio frequency integrated circuits, voltage-controlled oscillators**

I. Introduction

Continuing advances in low-power RF circuits have been bringing communication functionality to an increasingly wide variety of electronic devices. While most commercially available connected devices have high-throughput wireless chipsets (e.g., smartphones, TVs, vehicles, etc.), not all applications require high data rates. In fact, there are a vast number of applications that have extremely low data rate requirements: temperature, biochemical, and environmental monitoring applications are but a few examples that require on the order of a few communicated packets every few minutes (or less).

Additionally, many of these ultra-low-data rate applications have extreme physical size and/or energy constraints. For example, operational lifetime is an important metric for implantable devices or autonomous sensors deployed in remote areas, as replacement of batteries can be both invasive and costly. Since RF circuits typically dominate the power budget of sensor nodes [1], [2], further reduction of the power burden of communication circuits can help to enable many envisioned application areas that are not realizable in practice today.

Most recent work in low-power RF circuits describe excellent RF performance while requiring only on the order of a few tens to hundreds of picojoules to send or receive a bit of information [3]–[5]. Such radios are, however, typically optimized for sensor networks and body-area networks at data rates greater than 100 kb/s. Although energy-efficiency is a metric of great importance in nearly all applications, *average power* is a metric of greater importance for ultra-low-data-rate applications having extremely low energy storage and/or harvesting capacity. To achieve ultra-low average power, it is necessary to minimize not only active energy-per-bit, but perhaps more critically, standby power. At average data rates of 100 kb/s and above, minimizing standby power is often not a priority; as a result, such designs typically do not scale well down to ultra-low data rates.

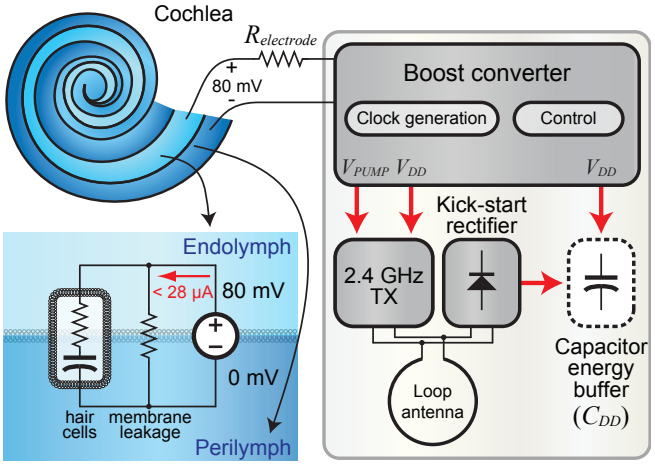


Fig. 1. Architecture of the endocochlear potential harvesting, sensing, and communicating system.

This paper presents a radio transmitter that is designed for energy harvesting applications that can only extract a *total* of approximately a nanowatt of power. Although there are several excellent designs that achieve very low radio standby power [6]–[8], there are few, if any, existing radio transmitters that consume below 200 pW – the radio power budget of this work after taking into account other system components.

The specific application targeted in this work is a system that harvests energy from the endocochlear potential located within the inner-ear of mammals [9]. A system block diagram is shown in Fig. 1. Here, current is extracted from the cochlea through a set of electrodes. Since the voltage of the source is low (typically between 70-100 mV), a boost converter is used to process the energy up to a higher voltage (typically

between 0.7-1.2 V), which is directly dumped onto capacitor C_{DD}. As more energy is extracted from the cochlea, it is continually buffered onto C_{DD}, forcing its voltage, V_{DD}, and as a result its stored energy, to rise. When sufficient energy has been stored on C_{DD}, the 2.4 GHz radio is enabled to quickly transmit a packet, then return to its ultra-low-power standby mode. Since the endocochlear potential is too low to directly start-up CMOS electronics, the loop antenna used by the transmitter is shared with a kick-start rectifier [10], used to initialize the charge on C_{DD} at system start-up.

The overall vision of the endocochlear potential harvesting work is described in [9]; details of the communication system are described in this paper. Note that although the targeted application is rather unique and specific, the techniques presented in this paper can be applied to many other applications requiring sub-nanowatt power budgets.

II. Transmitter Architecture

To achieve ultra-low standby power while maintaining high active energy efficiency, a low-complexity transmitter architecture with a minimum number of inherently high-leakage RF stages should be considered. With that in mind, this work employs a direct-RF power oscillator. The oscillator, shown in Fig. 2, is designed as a single-stage RF circuit by utilizing an on-board loop antenna that, due to anatomical size constraints, is electrically small at 2.4 GHz, and can therefore act as a high-Q inductive element in the resonant LC tank of the oscillator itself [11]. Such a topology performs automatic impedance matching with the antenna, and as a result, eliminates the need for an additional output buffer or power amplifier, thereby minimizing the number of high-leakage RF stages.

The power oscillator, whose core consists of the cross coupled NMOS pair of M1 and M2, is biased at their drains by a center tap on the loop antenna, and at their sources by a tail current source. The current source employs six binary-weighted transistors that are used to provide current (and as a result, radiated output power) programability. The tail transistors specifically use high-V_t devices that are driven by a full-swing charge pump voltage (V_{PUMP}, which is roughly double V_{DD}) in order to decrease the standby leakage power of the power oscillator by upwards of 300X over nominal-V_t devices operating at V_{DD} for equivalent on-conduction. OOK modulation is achieved by dynamically switching the tail sources on-and-off at the instantaneous data rate.

Since the loop antenna is electrically small, its radiation efficiency (and its inductance) increases with the physical size of the antenna. Due to the presence of parasitic capacitances (denoted by $C_{parasitic}$ in Fig. 2) that resonate with the loop antenna, there exists an upper limit to antenna size (and as a result, radiation efficiency) beyond which the oscillator will only operate below 2.4 GHz. As a result, it is imperative to minimize $C_{parasitic}$ through careful design in order to maximize the antenna performance (subject to application-specific size constraints). For example, rather than employing low-leakage high-V_t devices, transistors M1 and M2 are implemented with nominal-V_t devices to reduce their parasitic

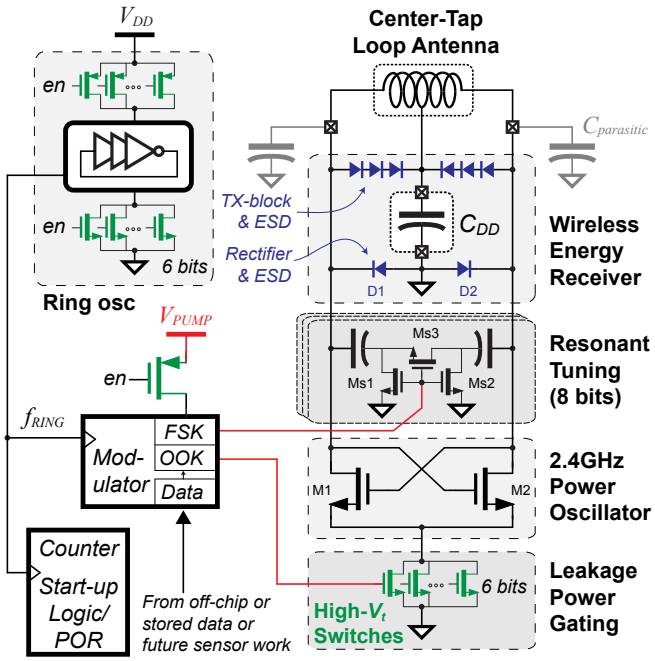


Fig. 2. Architecture of the direct-RF power oscillator with supporting circuitry.

capacitance by 10X for an equivalent drive-current at 2.4 GHz. Since the tail devices dictate the leakage of the entire stage anyways, this is a worthwhile design decision.

The center frequency of the power oscillator is tuned downward from its maximal frequency set by parasitics through a resonant tuning capacitive DAC, implemented primarily through 5 bits of binary-weighted MIM capacitors, totaling approximately 300 fF. A separate 3-bit sub-ranging DAC using custom-designed MOM capacitors is used to provide fine frequency control, with 0.25 fF switchable at the LSB. Coarse FSK modulation is achieved by dynamically reconfiguring the main DAC, while MSK modulation is achieved via the sub-ranging DAC. A differential switch design is employed by including transistor Ms3, reducing the parasitic capacitance of the DAC (which lumps directly into $C_{parasitic}$) for an equivalent Q. Additionally, the DAC is activated by full-swings signals at voltage V_{PUMP}, increasing the worst-case DAC Q by over 3X.

OOK and FSK signals are derived from a modulation block that is clocked by an on-chip ring-oscillator. The digital circuitry employs full-custom design, using standard cells that mix high-V_t and nominal-V_t transistors according to performance and energy requirements. For example, the ring oscillator is designed with nominal-V_t transistors for the inverting elements to minimize CV^2f active power, while being current starved with high-V_t devices to minimize standby leakage power. Six bits of current starving is used to ensure that the desired range of modulations frequencies can be achieved, even under severe PVT variation. Nearly all remaining circuitry is power gated using high-V_t devices at voltage V_{PUMP} (for super-cutoff operation), savings upward

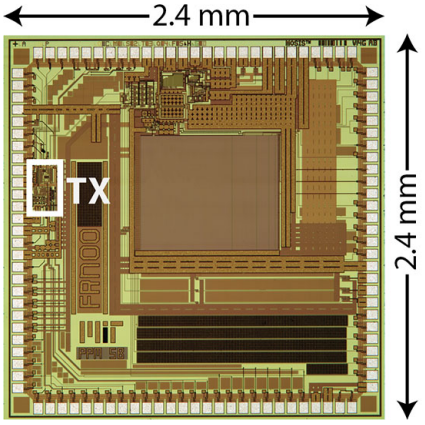


Fig. 3. Die photograph of the chip used to harvest energy from the endocochlear potential.

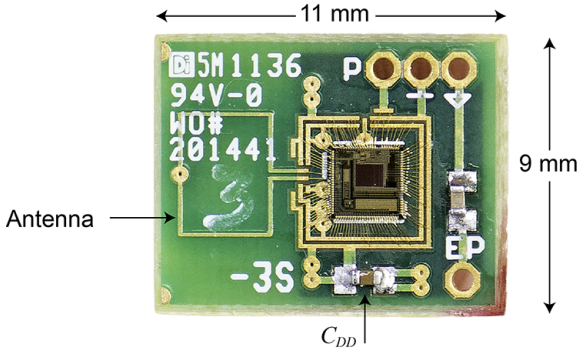


Fig. 4. Photograph of the chip-on-board package (the protective epoxy covering the chip is not shown for clarity).

of 4000X in leakage current from the V_{DD} supply, and 20X from the V_{PUMP} supply.

Given the center-tapped antenna architecture, the wireless energy receiving circuit for system kick-start requires only two diodes, D1 and D2, to create a full bridge rectifier. Interestingly, no area penalty is incurred by the rectifier, since D1 and D2 are already required for ESD protection purposes. Since the antenna is already implemented for the transmitter, kick-start functionality therefore comes for "free", with no additional area or parasitic capacitance. Note that due to the presence of RF waveforms biased around V_{DD}, three diodes must be connected in series for positive-rail ESD protection to prevent rectification of the outgoing RF signal itself.

III. Measurement Results

The transmitter was integrated together with the boost converter on a single chip that was fabricated in a 0.18 μm CMOS process. A die photo is shown in Fig. 3. The chip was directly wirebonded to a PCB containing the loop antenna and capacitor C_{DD} (Fig. 4). Since the antenna is a fixed part of the design, the direct RF output is not available to measure. Instead, unless otherwise specified, all RF measurements were performed by placing a $\lambda/4$ whip antenna a few centimeters away from the board.

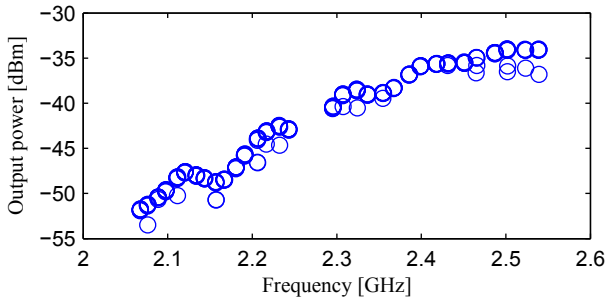


Fig. 5. Measured center frequency tuning and associated output power range, achieved by tuning the 8bit capacitive DAC.

Technology	0.18 μm	**Standby power** (0.8 V)	39.7 pW
Core area	0.035 mm^2	**Active power** (0.8 V)	191 μW
Supply	0.7–1.2 V	**Active E/bit** (5 Mb/s)	38 pJ/bit
Inst. data rate	1–10 Mb/s	**Average power** (1 b/s)	78 pW
Phase noise	-105 dBc/Hz	**Max output power** (1 V)	-20 dBm

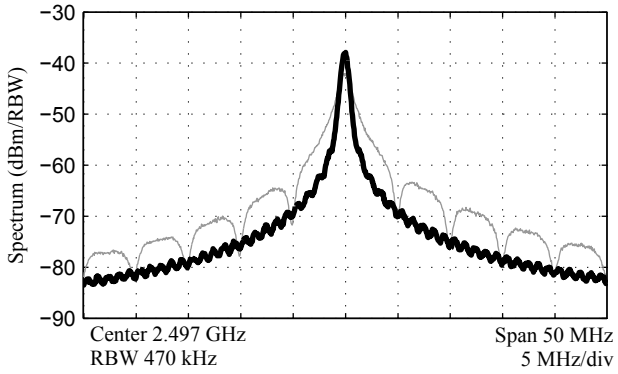
TABLE I
Summary of Chip Results

With the on-board 3x4 mm^2 antenna, the power oscillator achieved a tuning range of between 2.07-2.54 GHz, covering the ISM band at 2.4 GHz, as well as the MBAN band just below 2.4 GHz. As shown in Fig. 5, the radiated output power of the power oscillator increased with frequency, as expected for an electrically small antenna. At a distance of 1 m in a standard indoor environment, the maximum measured output power (with V_{DD} = 1 V) was approximately -60 dBm. These measurement together suggest that the maximum radiated output power of the transmitter was approximately -20 dBm. The measured output spectra for OOK and FSK/MSK modulation at two separate data rates are shown in Figs. 6(a) and 6(b), respectively. The power oscillator achieved a phase noise of -105 dBc/Hz at a 1 MHz offset.

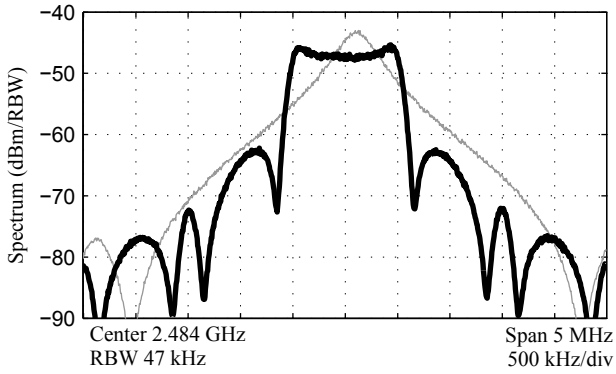
In active mode with V_{DD} = 0.8 V and a data rate of 5 Mb/s, the transmitter consumed 191 μW and 374 μW for OOK and FSK modulations, respectively. This resulted in an active energy efficiency of 38 pJ/bit and 75 pJ/bit for OOK and FSK, respectively. In standby mode at V_{DD} = 0.8 V, the transmitter was measured to consume 39.7 pW. As shown in Fig. 7, the transmitter achieved a startup time of 180 ns, contributing minimal energy during duty-cycled operation. Thus, at an *average* data rate of 1 b/s (for e.g., one 60-bit packet transmitted once per minute), the radio consumed an average of 78 pW, which is over 100X lower than previous work based on published standby and active power consumption numbers (assuming minimal startup overhead) [6]–[8]. Fig. 8 illustrates the measured standby power of the chip across various supply voltages. A summary of transmitter results is shown in Table I.

IV. Conclusion

By implementing a low-complexity architecture together with aggressive leakage management techniques, the transmitter presented in this paper was able to achieve both a standby



(a) OOK modulation at 1 Mb/s (dark) and 10 Mb/s (light).



(b) FSK modulation at 1 Mb/s (dark) and near-MSK 2.5 Mb/s (light).

Fig. 6. Measured spectra taken using a $\lambda/4$ whip antenna a few centimeters from the on-board loop antenna.

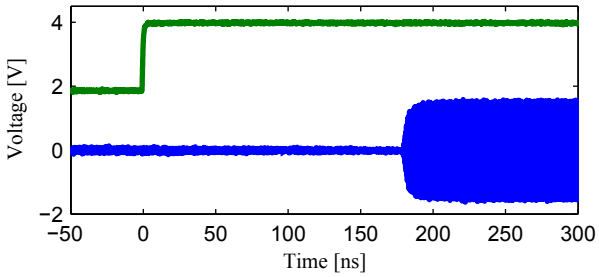


Fig. 7. Measured transient response, showing a 180 ns startup time between an enable signal and RF output.

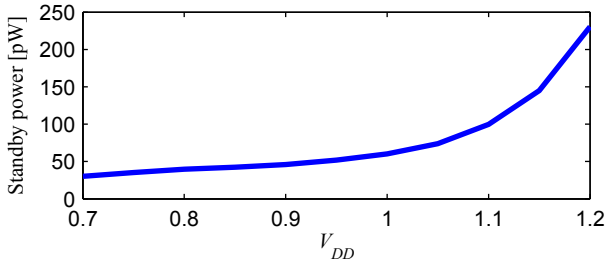


Fig. 8. Measured standby power of the transmitter for various supply voltages.

and average power consumption that is orders of magnitude lower than previous work. Instantaneously, the transmitter consumed 191 μW at 5 Mb/s during OOK modulation; however through extreme duty-cycling down to an average data rate of 1 b/s, the transmitter consumed only 78 pW. The transmitter was implemented in an area-efficient manner, occupying only 0.035 mm^2 of on-chip area, included a zero-overhead wireless kickstart circuit. By using a single-stage, direct-RF architecture that performed automatic impedance matching with an on-board 3x4 mm^2 antenna, the total size of the system is sufficiently small for implantable and other size-constrained applications.

Acknowledgments

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