A 440pJ/bit 1Mb/s 2.4GHz Multi-Channel FBAR-based TX and an Integrated Pulse-shaping PA

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Abstract

A 2.4GHz TX in 65nm CMOS defines three channels using three high-Q FBARs and supports OOK, BPSK and MSK. The oscillators have -132dBc/Hz phase noise at 1MHz offset, and are multiplexed to an efficient resonant buffer. Optimized for low output power ≈ -10dBm, a fully-integrated PA implements 7.5dB dynamic output power range using a dynamic impedance transformation network, and is used for amplitude pulse-shaping. Peak PA efficiency is 44.4% and peak TX efficiency is 33%. The entire TX consumes 440pJ/bit at 1Mb/s.

Introduction

Body Area Networks (BANs) for continuous health monitoring applications require radios that are both reliable and energy efficient in order to minimize device size and extend battery lifetime. Due to short transmit distances and an energy-asymmetric star topology, a low output power of -10dBm is sufficient for the sensor node [1]. Low PA power consumption places stringent power constraints on LO generation and modulation to maintain high overall TX efficiency. Recent work shows that high-Q direct-RF resonators, such as FBAR and SAW, provide low-power and stable LOs [2, 3], avoiding slow-starting, power-hungry PLLs. Low tuning range, however, limits its operation to a single channel. Typical PAs are not optimized for low output power, and this presents additional challenges.

This work proposes a high-Q RF resonator-based frequency generation architecture that scales to multiple channels by multiplexing resonators. A three-channel FBAR-based TX operating in the 2.4GHz ISM band demonstrates the idea. Additionally, a PA optimized for low output power is proposed, with an integrated tunable impedance transformation network capable of amplitude pulse-shaping for improved spectral efficiency.

Multi-Channel Transmitter Architecture

Fig. 1 shows the TX architecture. Three FBAR oscillators are multiplexed to an efficient resonant buffer which directly drives the PA. The buffer stage also incorporates matched delays with inverted phase to provide BPSK modulation. Since the output power is low, overall TX efficiency is critical, and informs the design choices for LO generation, modulation, and channel multiplexing. A low voltage design (0.7V) coupled with rail-to-rail swing on all RF nodes is used for improved power efficiency. Full swing on the oscillator minimizes short-circuit current in the buffers, while full swing at the input of the PA maximizes overdrive. The TX is designed for a datarate of 1Mb/s and supports three simple modulation schemes: OOK, BPSK and MSK, all with pulse-shaping capability.

Fig. 1 also shows the schematic of a Pierce oscillator [2] used for one channel. This inverter-based circuit provides rail-to-rail output swing and reduces power consumption by 2x over an NMOS-only implementation via current re-use. The oscillator consumes 150μW. A digitally controlled capacitor bank, C_{MSK}, tunes the oscillator center frequency over a 600kHz range with a 9.5kHz step-size, which is sufficient for 1Mb/s GMSK modulation. The measured phase noise at the antenna is -132dBc/Hz at 1MHz offset. The oscillators have a startup time $<4\mu$s, permitting aggressive TX duty-cycling.

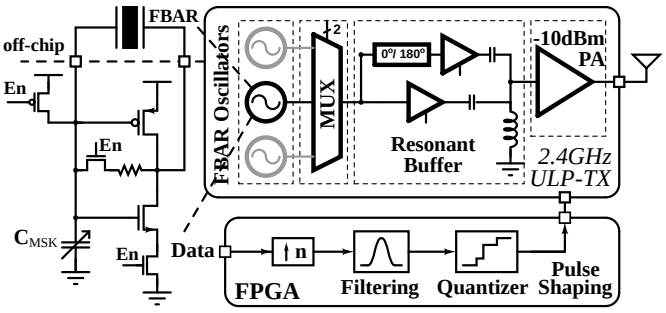

Fig. 1. TX architecture with the FBAR oscillator of one channel

The outputs of the three FBAR oscillators are multiplexed using transmission gates onto a resonant buffer that isolates the oscillator from the variable Miller capacitance of the PA. The low input-capacitance of the buffer also minimizes loading on the oscillator. Resonance of the large PA gate capacitance with an on-chip inductor minimizes power consumption since the buffer only needs to compensate losses in the tank. As pulse-shaping is handled by the PA and linearity is not a concern, the buffer is implemented as a CMOS inverter and gives rail-to-rail swing to the PA. Full-swing input from the oscillator leads to low short-circuit current. The buffer consumes 100μW. When compared to a non-resonant buffer, resonance results in greater than 2.5x lower buffer power, and 30% lower system power.

Integrated Pulse-Shaping Power Amplifier

The proposed push-pull PA is illustrated in Fig. 2. Transistors M1 and M2 are biased at $\approx V_{TN}$ and $\approx (V_{DD} + V_{TP})$ respectively with on-chip resistive-divider DACs to trade-off short-circuit current and on-resistance. With the PA driven strongly by rail-to-rail inputs from the buffer, drain node D has a full 0 to V_{DD} swing, which gives the highest PA efficiency. However, in order to radiate -10dBm, a 50Ω antenna requires only $200\text{mV}_{\text{p-p}}$ swing. To achieve this while also maintaining rail-to-rail swing at D, an impedance up-converter to $Z_L > 50\Omega$ is used. The push-pull topology is better than inductor-biased topologies (such as class E) since node D only requires a swing of V_{DD} (and not $2V_{DD}$) for maximum efficiency operation.

A fully-integrated tapped-capacitor matching network is used for the impedance up-conversion. Digitally tunable capacitors C_1 and C_2 are simultaneously varied to maintain resonance, while up-converting to various values of Z_L as shown by the governing equations and examples in Fig. 2. A 7.5dB output power tuning range is achieved with negligible increase in matching network complexity, while rail-to-rail swing at node D provides maximum efficiency in all these settings. In

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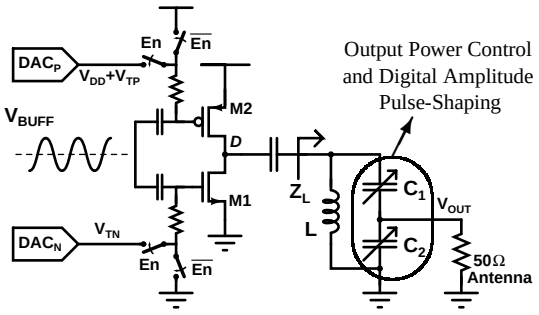

L (nH)	C_1 (fF)	C_2 (fF)	Z_L (Ω)	P_{OUT} (dBm)
6.44	960	1010	300+j0	-7
	850	1810	600+j0	-10
	780	2820	1200+j0	-13

$$Z_L \approx 50\left(1+\frac{C_2}{C_1}\right)^2 + j0$$
$$\omega^2 \approx \frac{C_1+C_2}{LC_1C_2}$$
$$P_{OUT} \approx \frac{V_{DD}^2}{8\Re(Z_L)}$$

Fig. 2. Integrated PA with pulse-shaping using dynamic impedance transformation and its governing equations

addition, these capacitor bank settings can be switched dynamically, at rates >10MHz, and are hence used for efficient amplitude pulse-shaping. This is opposed to a power-hungry linear mixer + PA approach. Traditional methods of efficient pulse-shaping like supply modulators [4] can be used in addition to this technique to expand the output power range even further.

Measurement Results

The TX is fabricated in a 65nm CMOS process. A 0.7V supply powers the RF circuits and a 1V supply powers the digital switches in the multiplexers and capacitor banks. Unless otherwise specified, all measurements reported are for a PA supply of 0.7V. The peak PA efficiency is 43% for an output power of −7dBm. When the PA operates at 0.5V, peak PA efficiency is 44.4% for an output power of −9.3dBm. Overall TX efficiency is plotted in Fig. 3 as the impedance transformation ratio is varied. At 0.7V PA supply, peak TX efficiency is 28.6% and at 1V, it is 33%, the highest for all frequency-stable transmitters with sub-mW outputs operating in the GHz frequencies (Fig. 3).

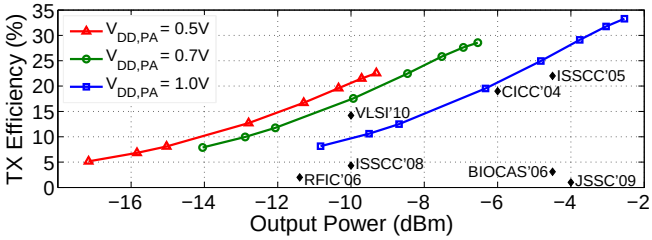

Fig. 3. Overall TX efficiency versus output power.

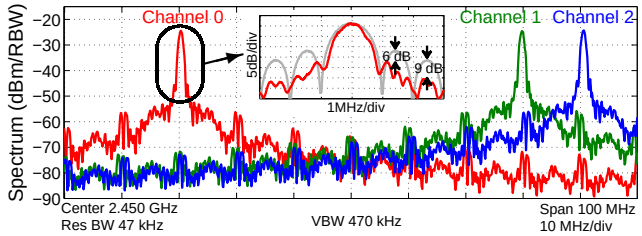

Fig. 4. Spectra of Gaussian pulse-shaped and phase-scrambled 1Mb/s OOK for the three channels measured from the chip

Fig. 4 shows the multi-channel capability of the TX. Spectra of 1Mb/s Gaussian pulse-shaped (α=0.3) phase-scrambled OOK (10x oversampling) of the three channels measured from the chip are superimposed. Spurs from the 10x oversampling are all below −30dBc. Pulse-shaping reduces the first sidelobe

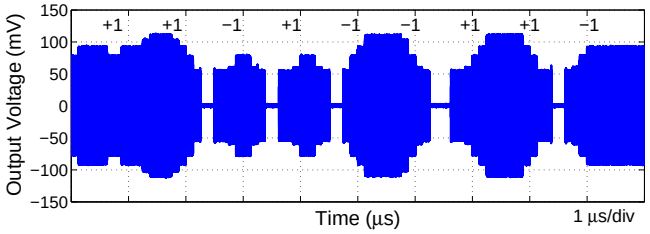

Fig. 5. 1Mb/s BPSK modulated waveform with SRRC filtering

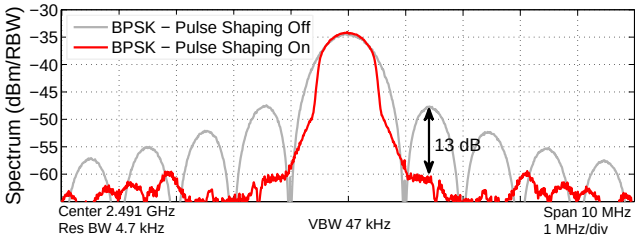

Fig. 6. 1Mb/s BPSK spectra with and without pulse-shaping

by 6dB and the second sidelobe by 9dB. At a −12.5dBm average output power, the TX consumes 440pJ/bit, which is lower than all resonator-based transmitters at GHz frequencies.

Measured transient waveform and spectra for 1Mb/s BPSK are shown in Figs. 5, 6. Square Root Raised Cosine (SRRC) filtering (β=0.3) at 8x oversampling suppresses the first sidelobe by 13dB. The TX consumes 530pJ/bit while transmitting −11dBm in this mode. In GMSK mode, the TX consumes 550pJ/bit at −10dBm output power. The digitally filtered GMSK modulation reduces the first sidelobe by 7dB and second sidelobe by greater than 20dB as compared to MSK.

Technology	65nm CMOS
Supply	0.7V (RF), 1V(Switch)
Num. Channels	3
Startup Time	$4\mu s$
Data Rate	1Mb/s
Phase Noise	-132dBc/Hz (1MHz off.)
PA Peak Eff.	44.4%
TX Peak Eff.	33%
P_{OUT}	-17dBm to -2.5dBm
Energy per bit and Average P_{OUT}	
OOK (Gauss.)	440pJ/bit at -12.5dBm
BPSK(SRRC)	530pJ/bit at -11dBm
GMSK	550pJ/bit at -10dBm

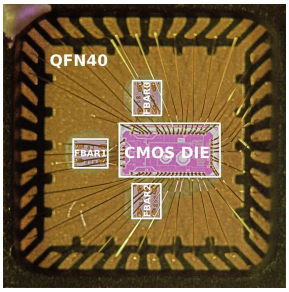

Fig. 7. TX performance summary and packaging photograph

Fig. 7 summarizes the TX specifications and shows the packaging photograph of the CMOS die co-packaged with three FBARs in a QFN40. The TX core occupies an area of $0.324mm^2$. The TX has also been used to successfully transmit packetized ECG data to a commercial receiver.

In conclusion, a TX architecture optimized for the short-distance link budgets of BANs is presented. The PA is optimized for operation at −10dBm with integrated pulse-shaping capability. High-Q FBAR based LO generation is extended to three-channel operation. Integrated on-chip resonators [5] will enable area-efficient expansion to larger number of channels.

References

[1] IEEE P802.15 TG6 Body Area Networks (BAN) draft standard, accessed Dec. 2011, http://www.ieee802.org/15/pub/TG6.html

[2] Y. Chee, et al., *Proc. Symp. VLSI Circuits*, pp. 43-44, Jun. 2006.

[3] M. K. Raja, et al., *Proc. A-SSCC'08*, pp. 341-344, Nov. 2008.

[4] F. Raab, et al., *Microwave Theory and Techniques, IEEE Transactions on*, vol. 50, no. 3, pp. 814-826, 2002.

[5] D. Weinstein, et al., *Nano Letters*, pp. 1234-1237, Apr. 2010.