Session 6 - Power Management Circuits and Architectures

# A 78%-Efficiency Li-ion-Compatible Fully-Integrated Modified 4-Level Converter with 0.01- 40mW DCM-Operation in 28nm FDSOI

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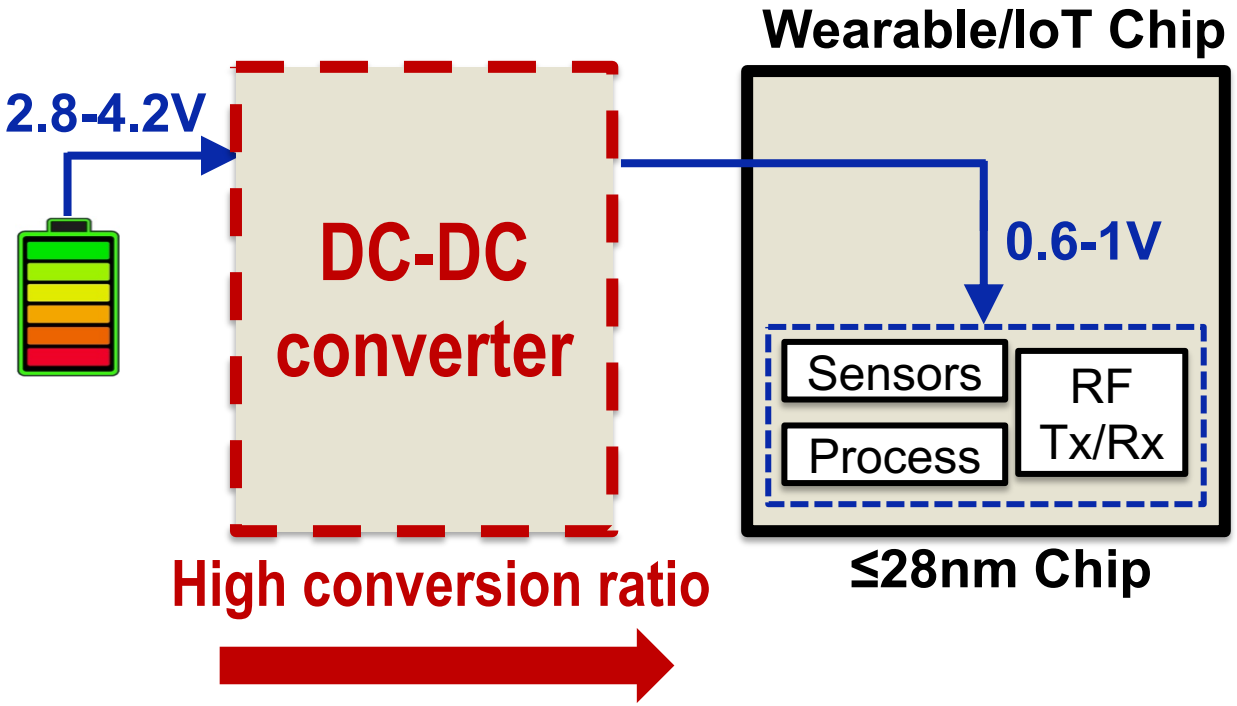
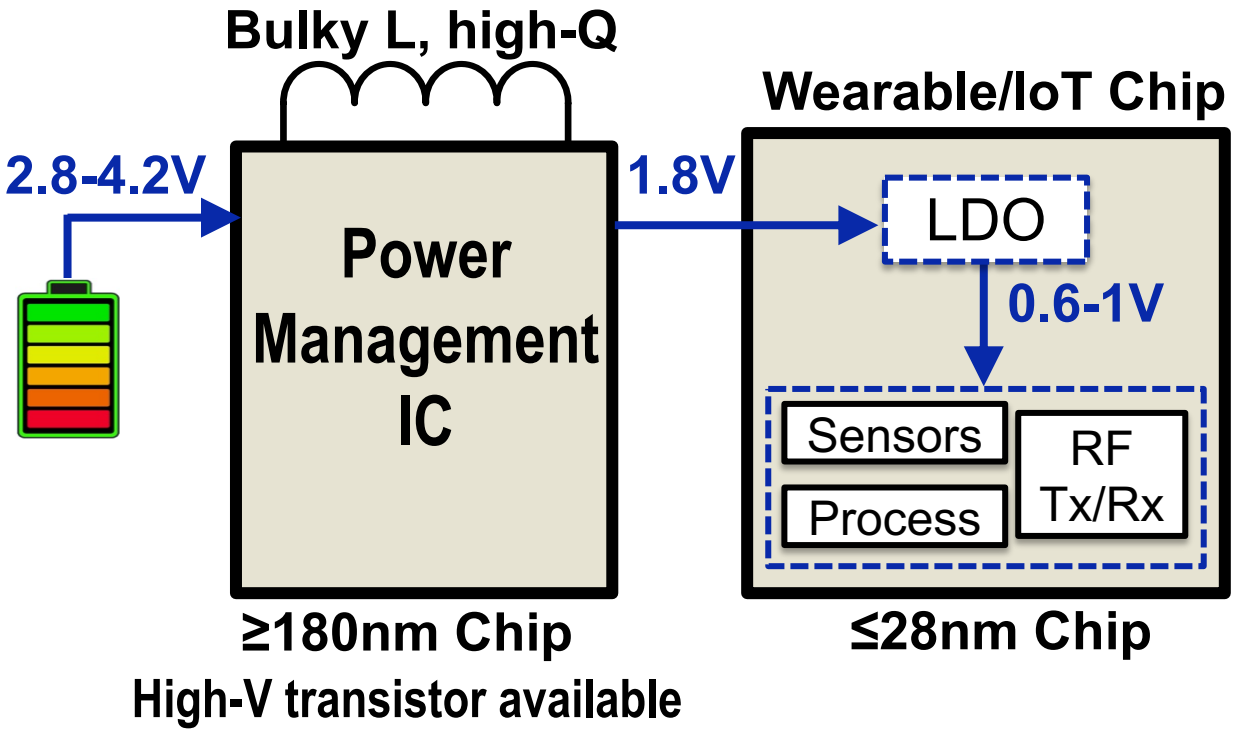
# Powering IoT and Wearables in Scaled-CMOS




Small wearable/IoT devices is implemented in scaled-CMOS and use Li-ion batteries as power supply

# Powering IoT and Wearables in Scaled-CMOS

## Conventional




Discrete PMIC is implemented in technologies that can handle the high battery voltage

# Powering IoT and Wearables in Scaled-CMOS

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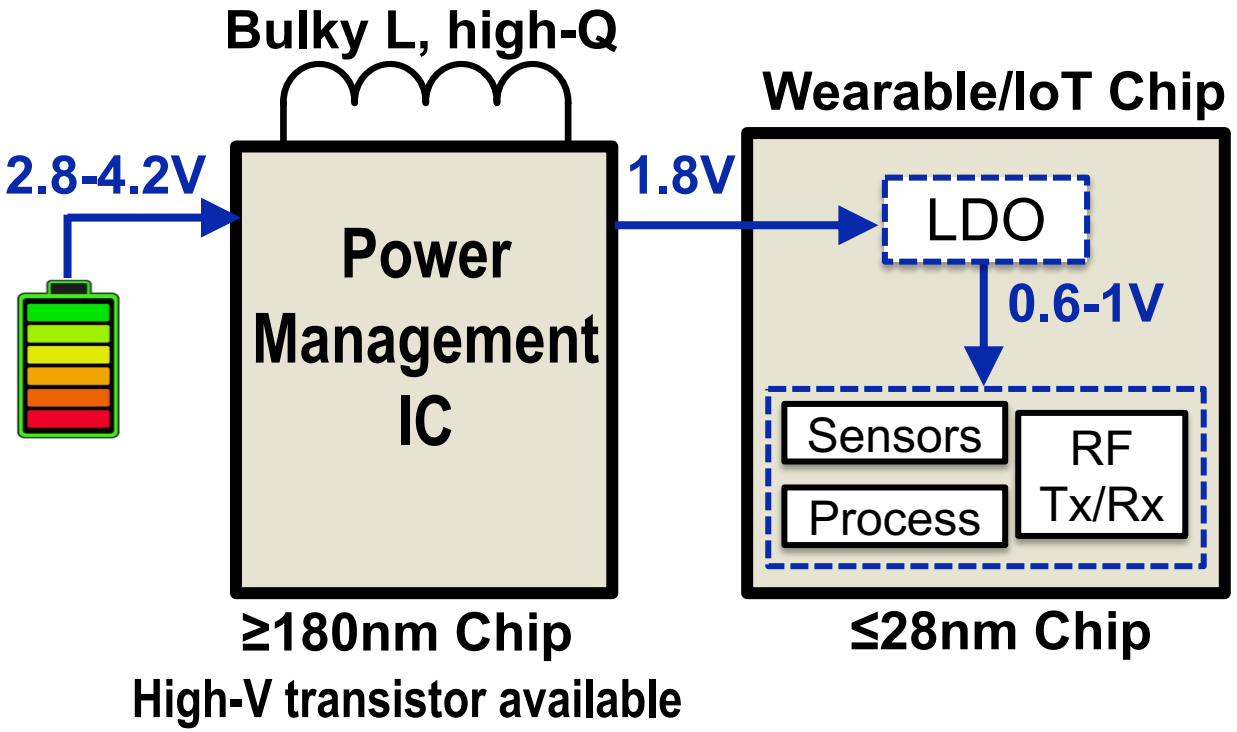


↑Area ↑PCB complexity/cost

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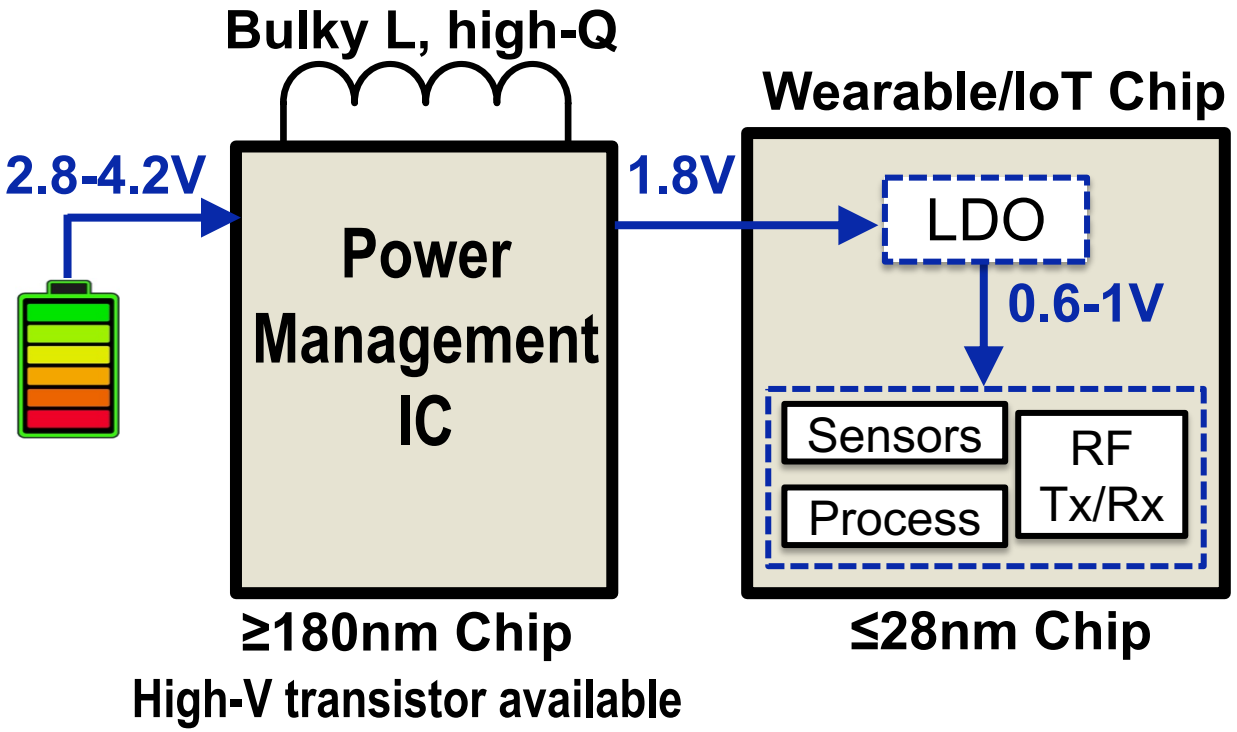
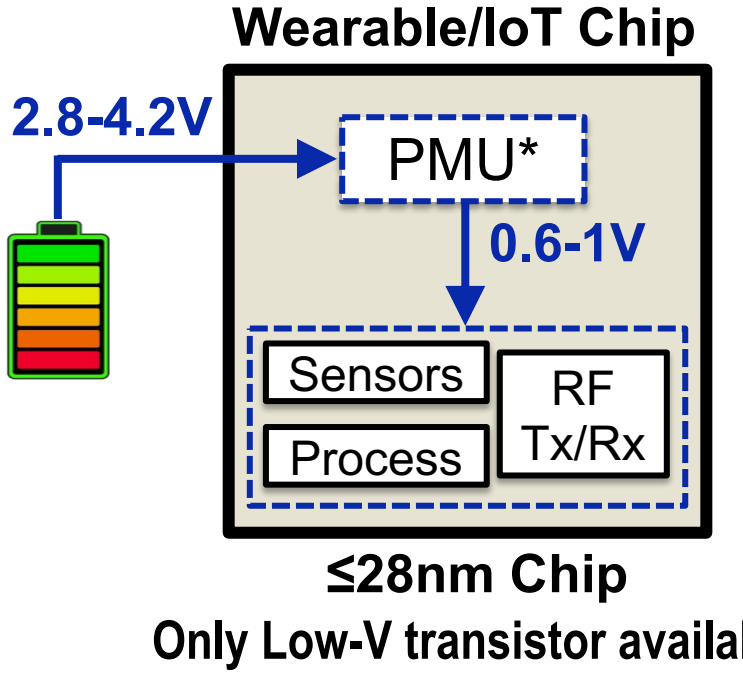



↑Area ↑PCB complexity/cost

## Goal




Small form factor
↓PCB complexity/cost

PMU* : Power Management Unit

# Li-ion Fully-Integrated PMU Challenges in 28nm FDSOI

Scaled-CMOS Challenges

Only Low-V transistors available

Transistors stacking required

- High switching & conduction losses
- Complex power-hungry drivers
- Many level shifters

**Poor efficiency**

Only Low-V capacitors available

Capacitors stacking required

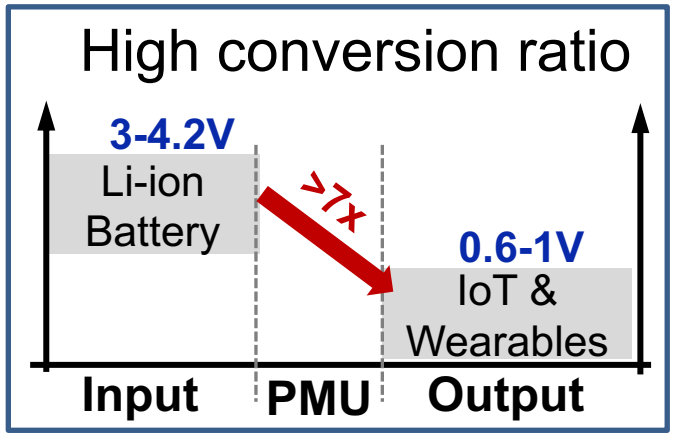
Large area

**Low power density**

Poor quality on-chip passives

- Large ESR, parasitic cap
- Low density

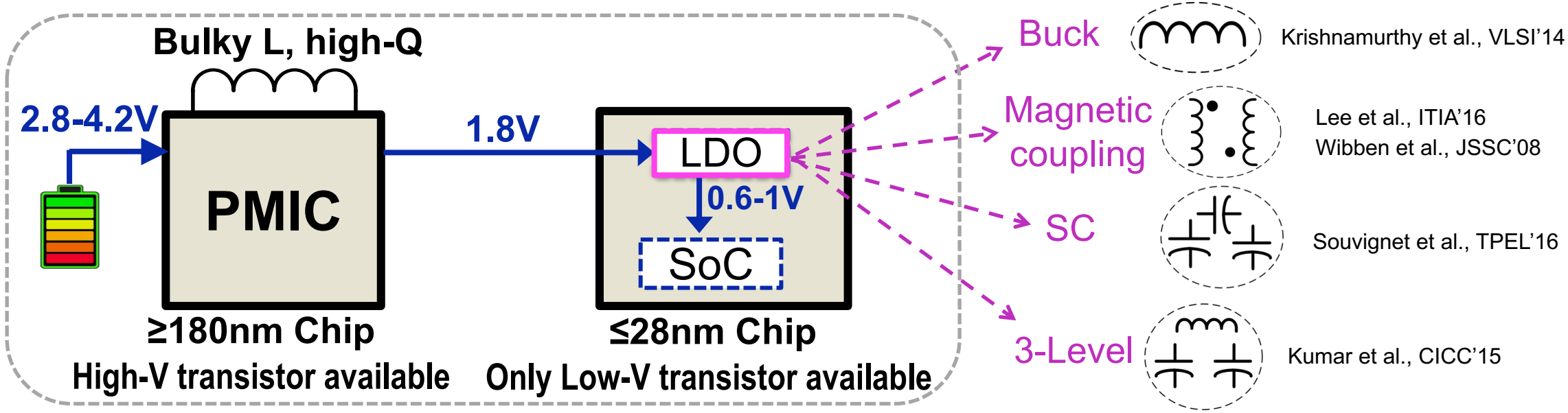
**Poor efficiency**
**Low power density**

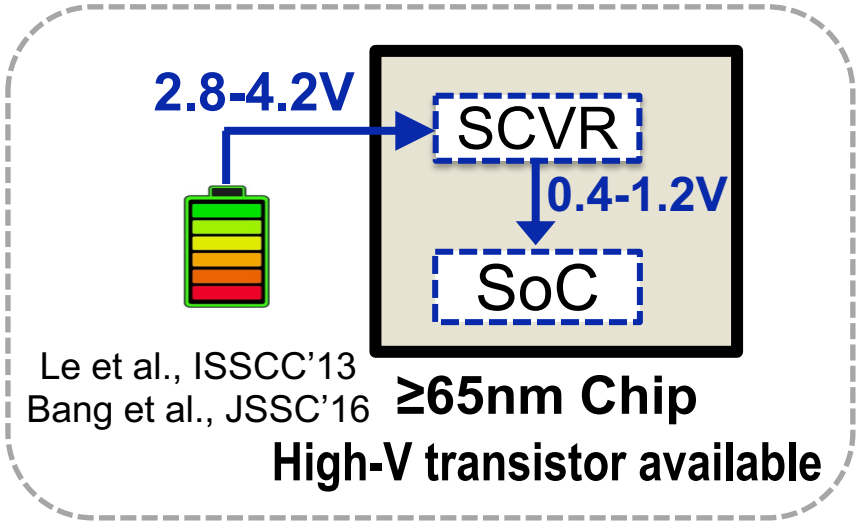


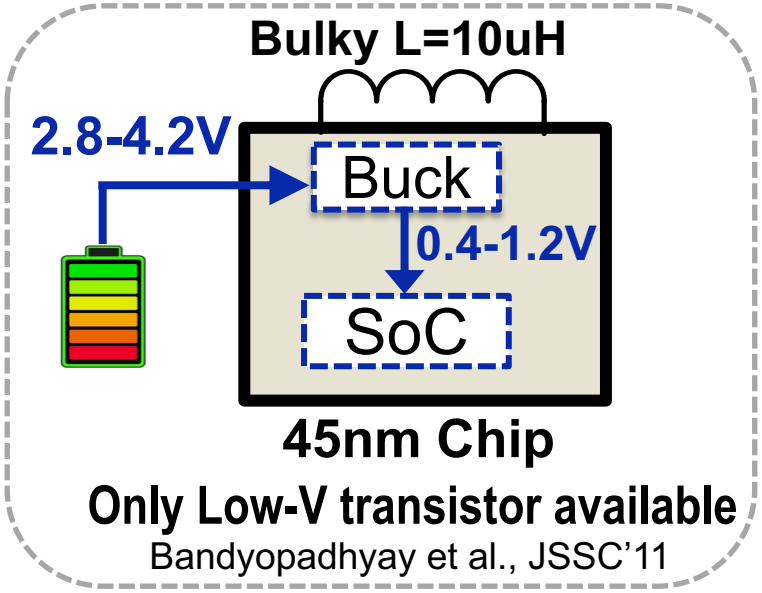
# Outline

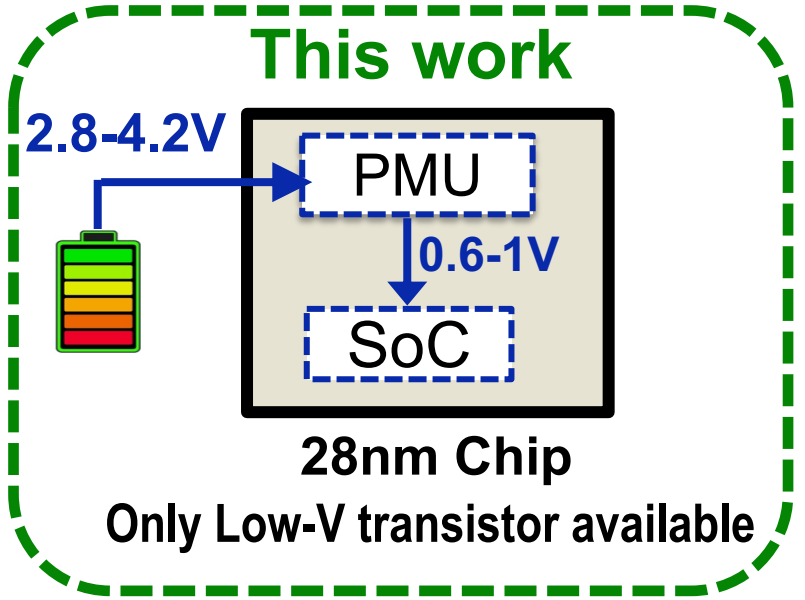
- Prior Work
- Proposed Hybrid Architecture
- Switching Phases of the Proposed Architecture
- Circuit Details
- Measurement Results
- Conclusion

# Prior Work

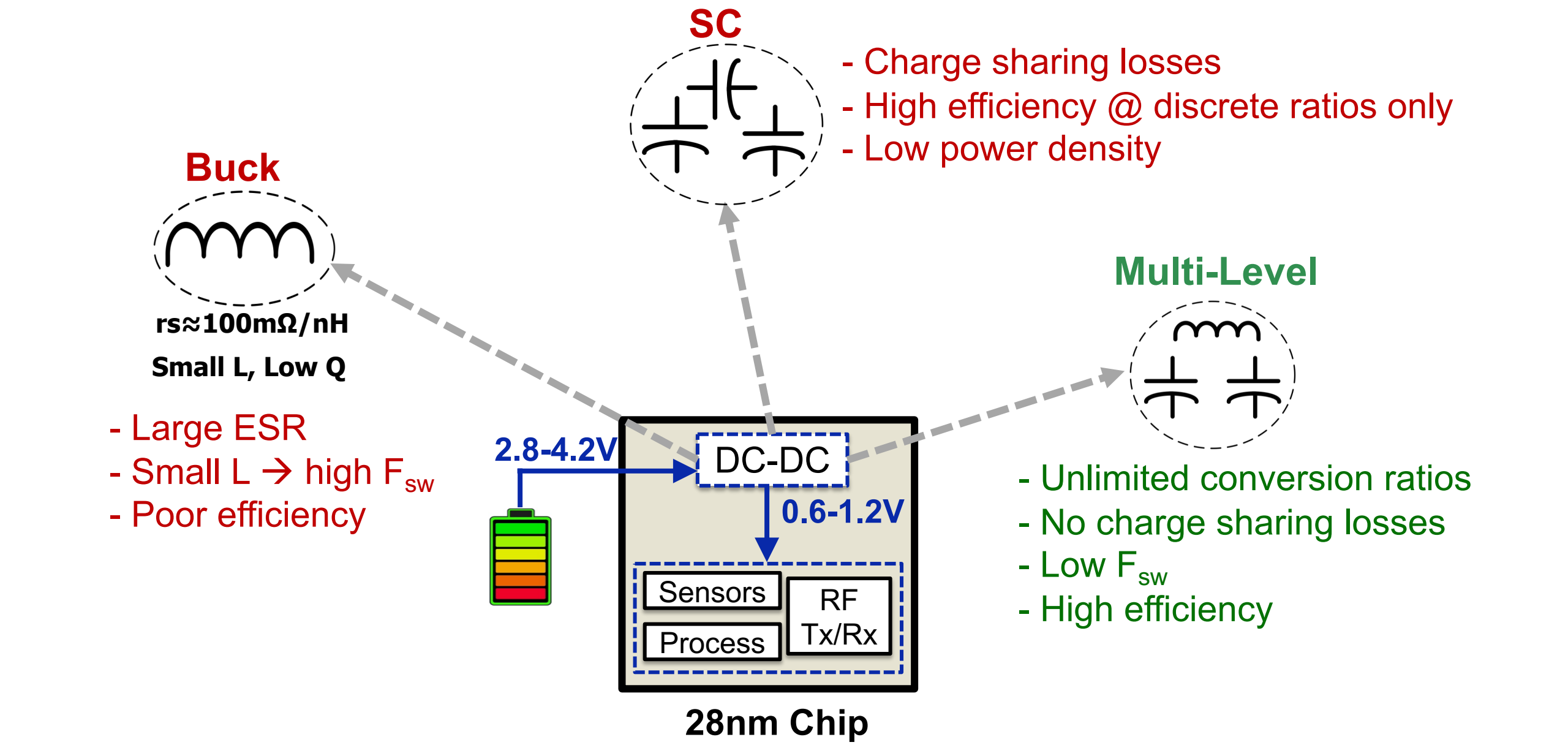

Bulky L, high-Q
2.8-4.2V
PMIC
1.8V
LDO
0.6-1V
SoC
≥180nm Chip
High-V transistor available
≤28nm Chip
Only Low-V transistor available
Buck
Krishnamurthy et al., VLSI'14
Magnetic coupling
Lee et al., ITIA'16
Wibben et al., JSSC'08
SC
Souvignet et al., TPEL'16
3-Level
Kumar et al., CICC'15


2.8-4.2V
SCVR
0.4-1.2V
SoC
Le et al., ISSCC'13
Bang et al., JSSC'16
≥65nm Chip
High-V transistor available


Bulky L=10uH
2.8-4.2V
Buck
0.4-1.2V
SoC
45nm Chip
Only Low-V transistor available
Bandyopadhyay et al., JSSC'11


This work
2.8-4.2V
PMU
0.6-1V
SoC
28nm Chip
Only Low-V transistor available

# Fully Integrated DC-DC Converter for $V_{in}$=2.8-4.2V



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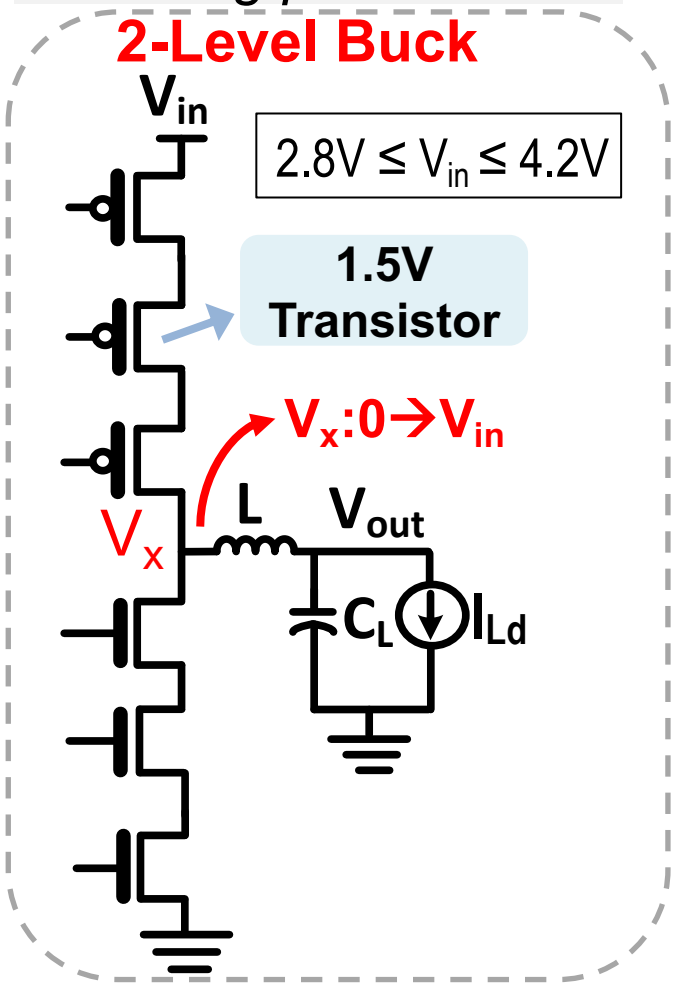
# Towards Fully-Integrated Li-ion PMU in Scaled CMOS

*Starting point:* Buck




***Small on-chip L, large ESR***

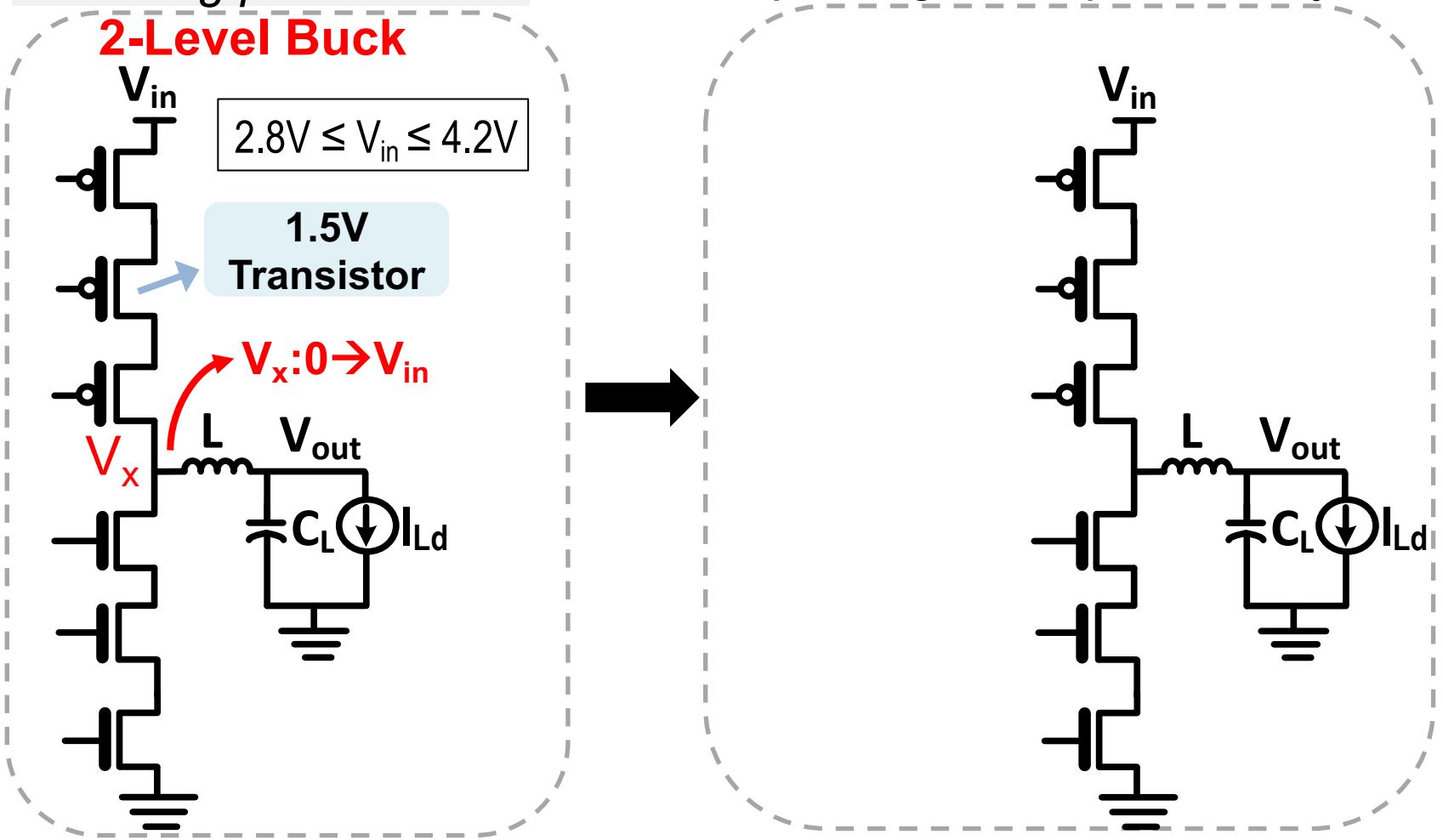
-High Switching & conduction losses

-Poor efficiency

# Towards Fully-Integrated Li-ion PMU in Scaled CMOS

*Starting point:* Buck

*Improving on-chip efficiency*




Stacking transistors is required anyway

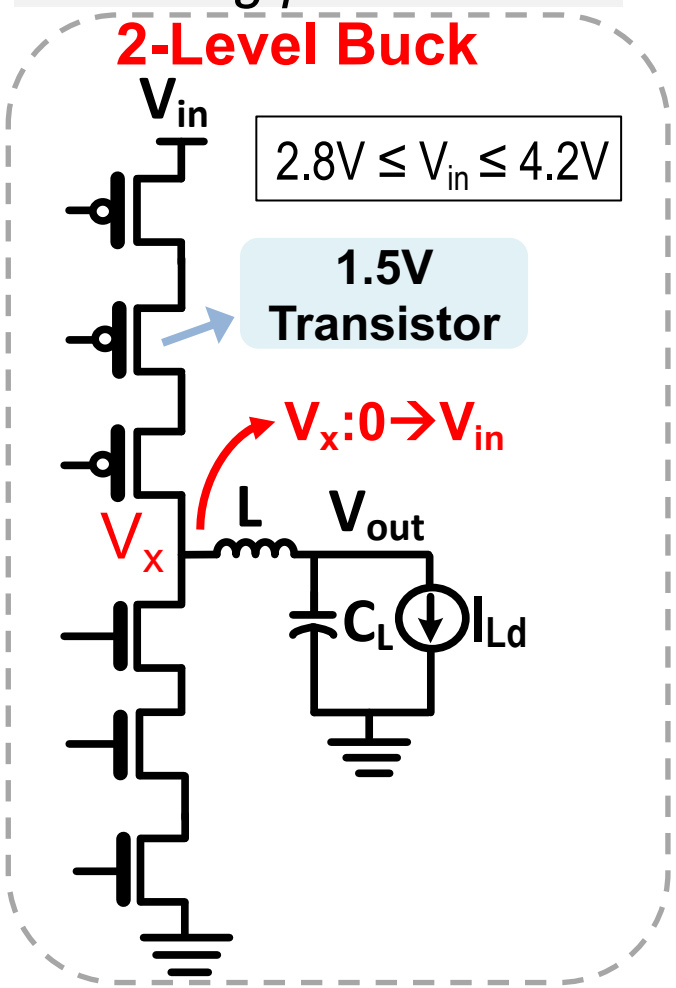
***Small on-chip L, large ESR***

-High Switching & conduction losses

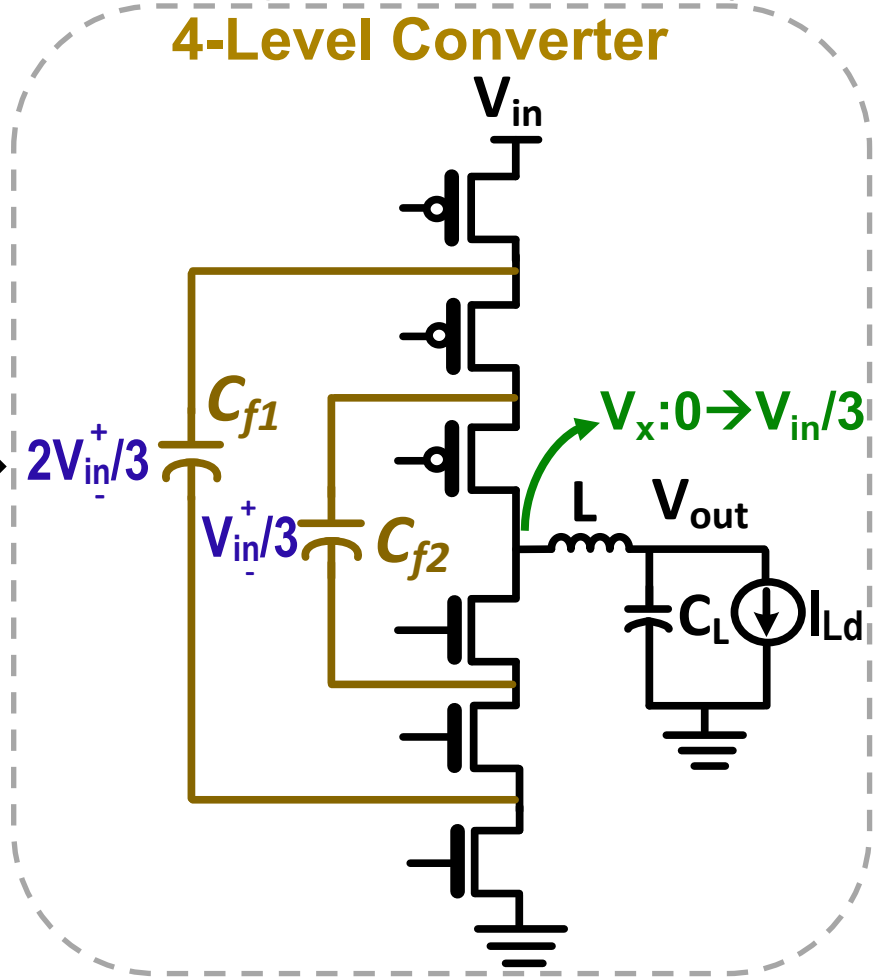
-Poor efficiency

# Towards Fully-Integrated Li-ion PMU in Scaled CMOS

*Starting point:* Buck




*Improving on-chip efficiency*




Stacking transistors is required anyway

***Small on-chip L, large ESR***

-High Switching & conduction losses

-Poor efficiency

***Reduced swing at Vx***

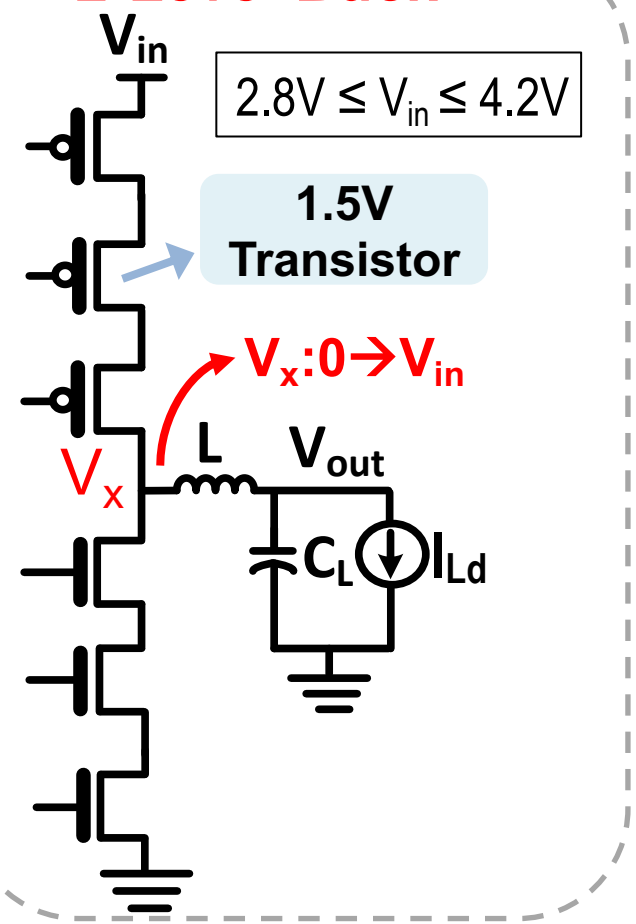
*$F_{sw}$ reduced by > 23x*

*& efficiency by up to 33%*

# Towards Fully-Integrated Li-ion PMU in Scaled CMOS

*Starting point:* Buck

**2-Level Buck**



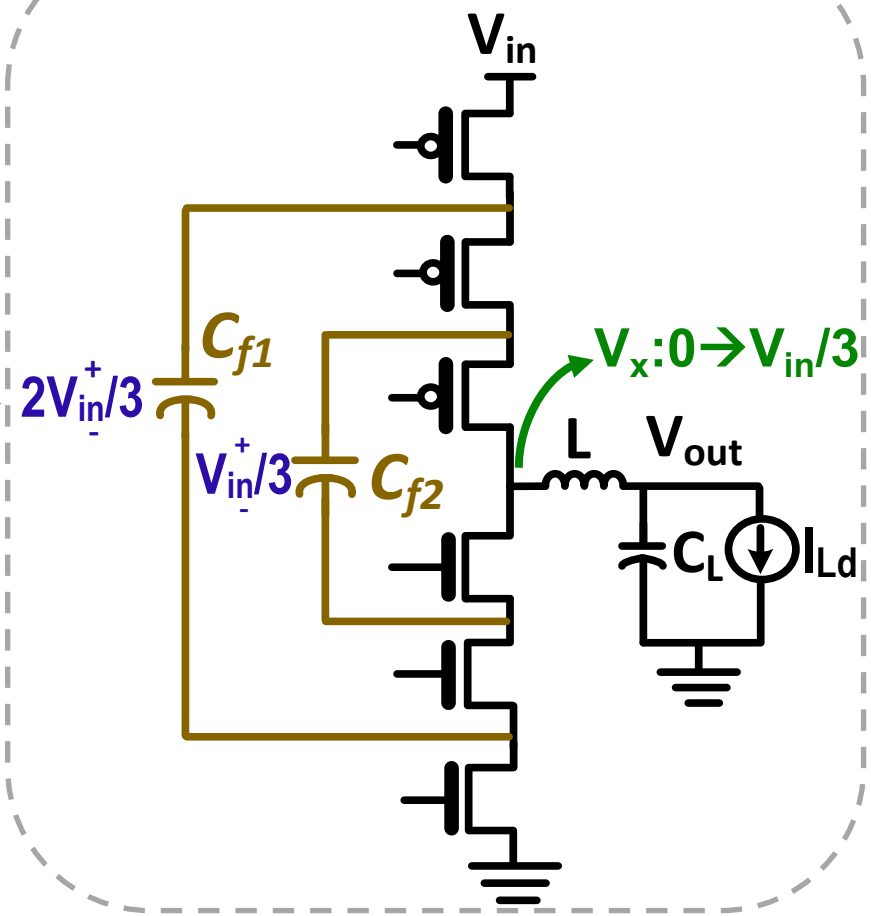

***Small on-chip L, large ESR***

-High Switching & conduction losses

-Poor efficiency

*Improving on-chip efficiency*

**4-Level Converter**




***Reduced swing at Vx***

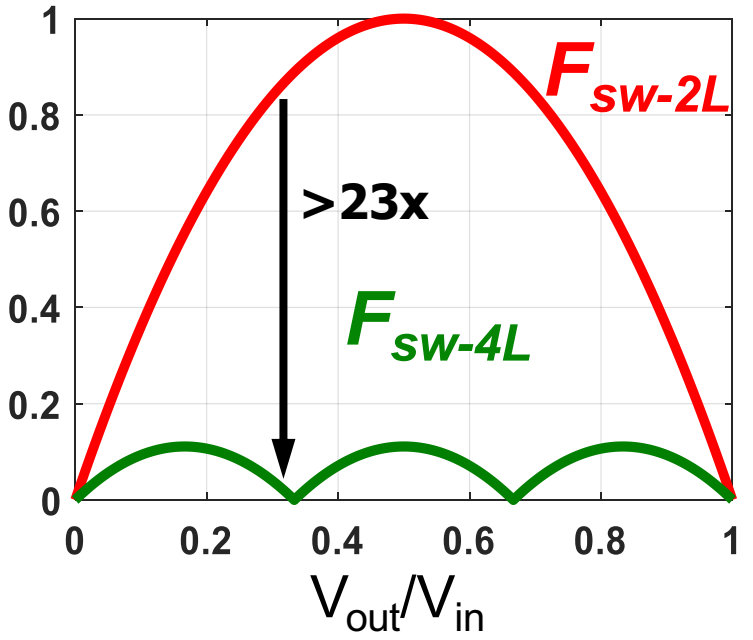
*$F_{sw}$ reduced by > 23x*

*& efficiency by up to 33%*

**DCM-operated**

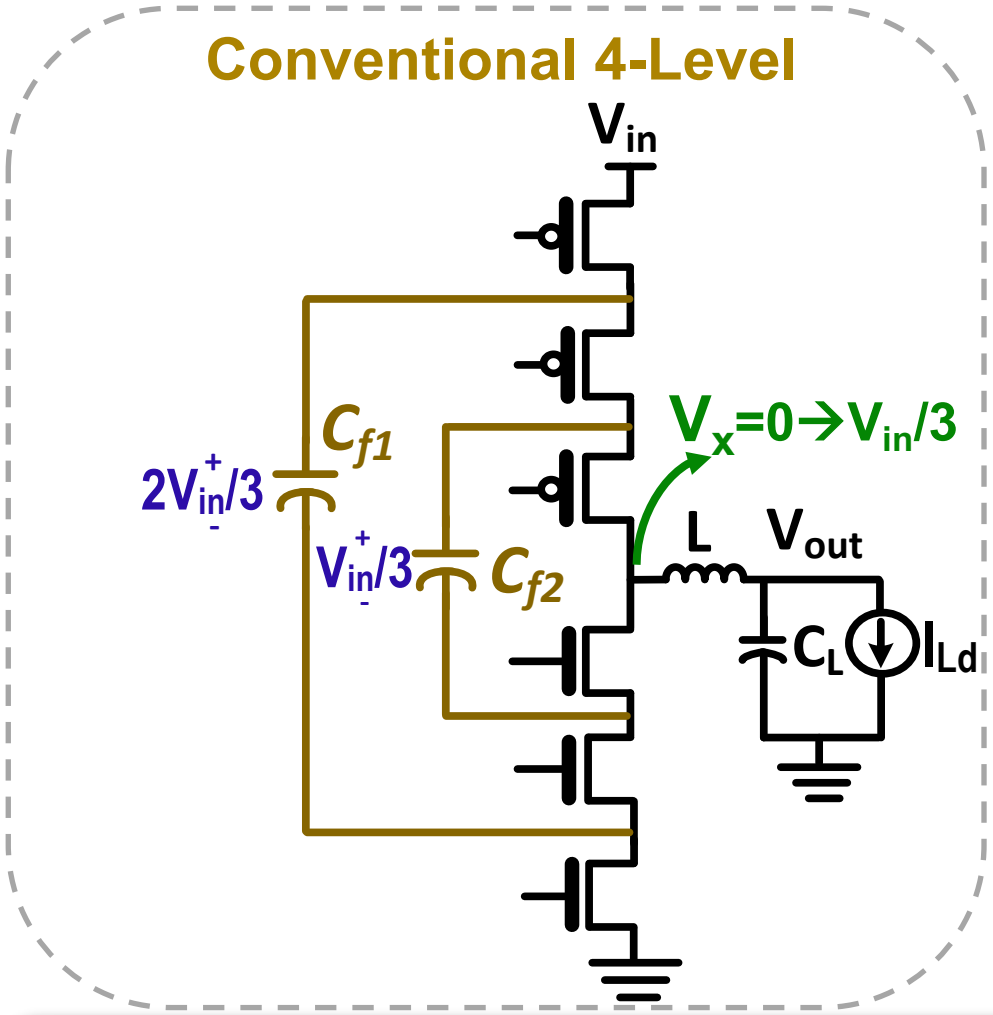
Constant $I_{pk}$

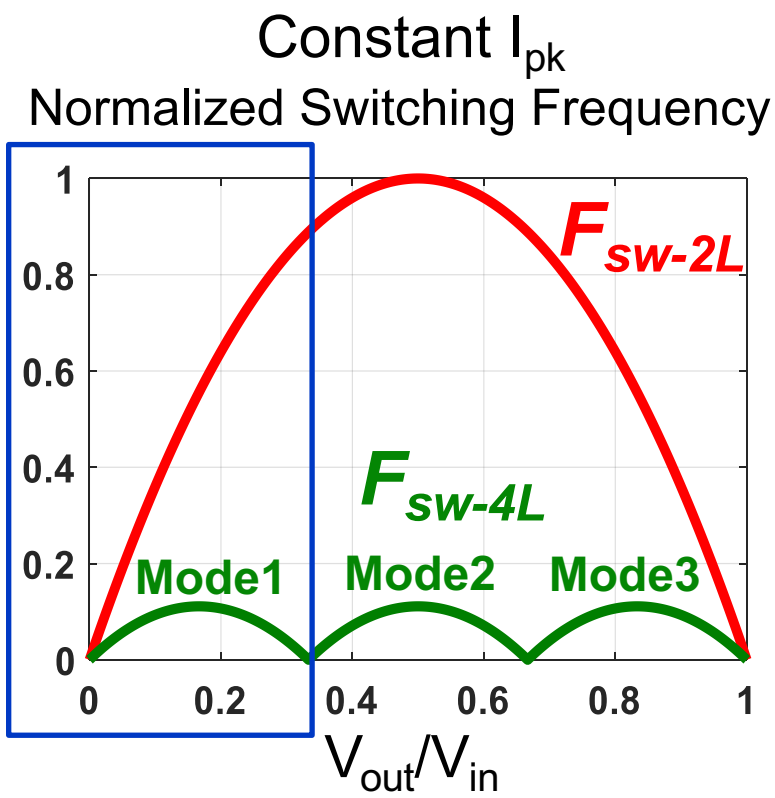
Normalized Switching Frequency




$$\frac{F_{sw\_4L}}{F_{sw\_2L}} = \frac{1/3 - V_{out}/V_{in}}{1 - V_{out}/V_{in}}$$

# 4-Level Converter Modes of Operation




$0 \le V_{out} \le V_{in}/3$

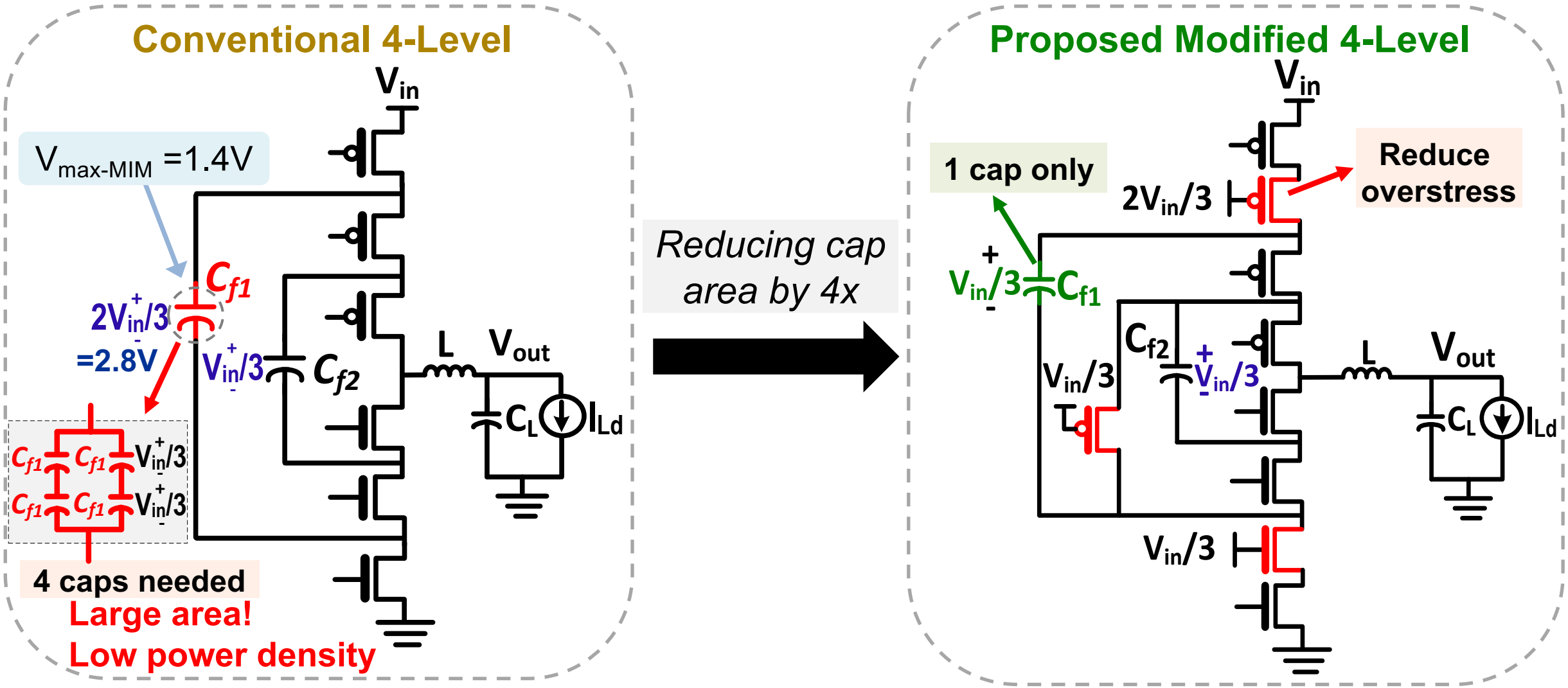
*Mode1*: $V_x = 0 \rightarrow V_{in}/3$

*Mode2*: $V_x = V_{in}/3 \rightarrow 2V_{in}/3$

*Mode3*: $V_x = 2V_{in}/3 \rightarrow V_{in}$

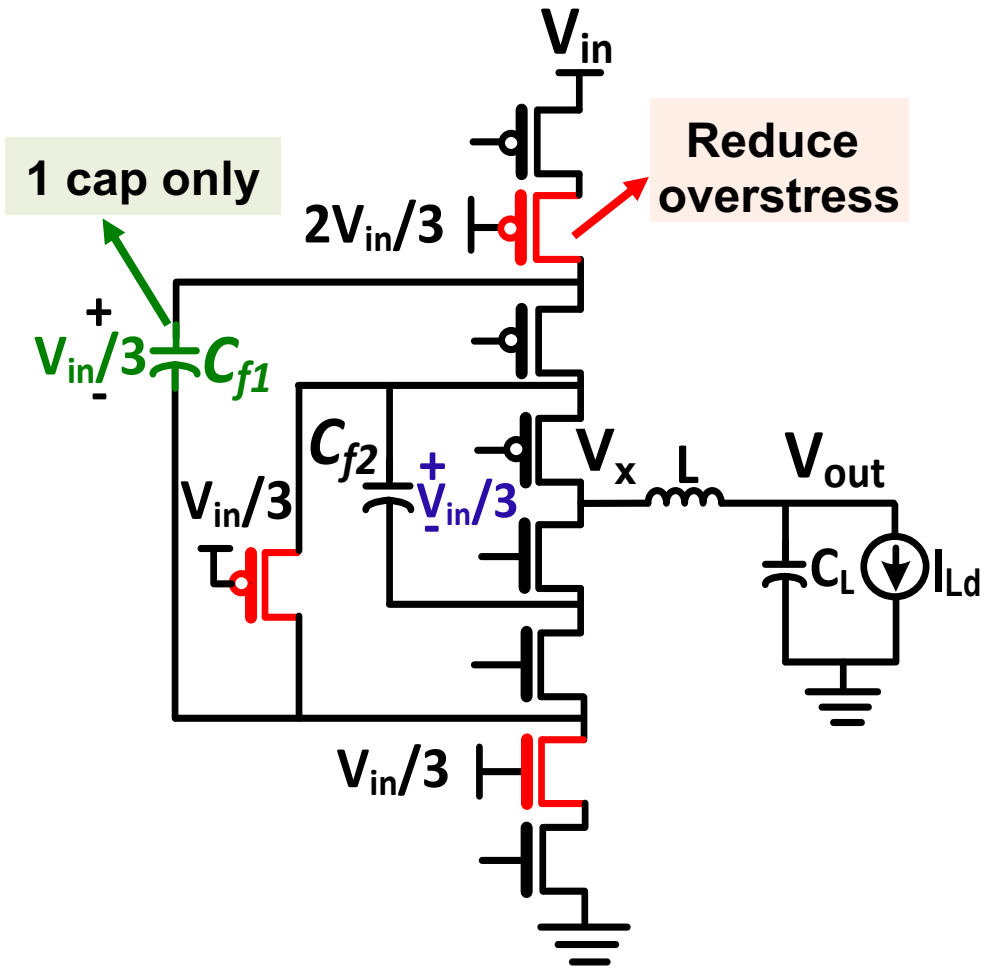
The converter operates only in a single-mode for:
$2.8 \le V_{in} \le 4.2$ & $0.6 \le V_{out} \le 1$

# Conventional 4-Level Converter Area Penalty




Changing the switching states of flying caps reduces the cap voltage stress

# Proposed Modified 4-Level Converter

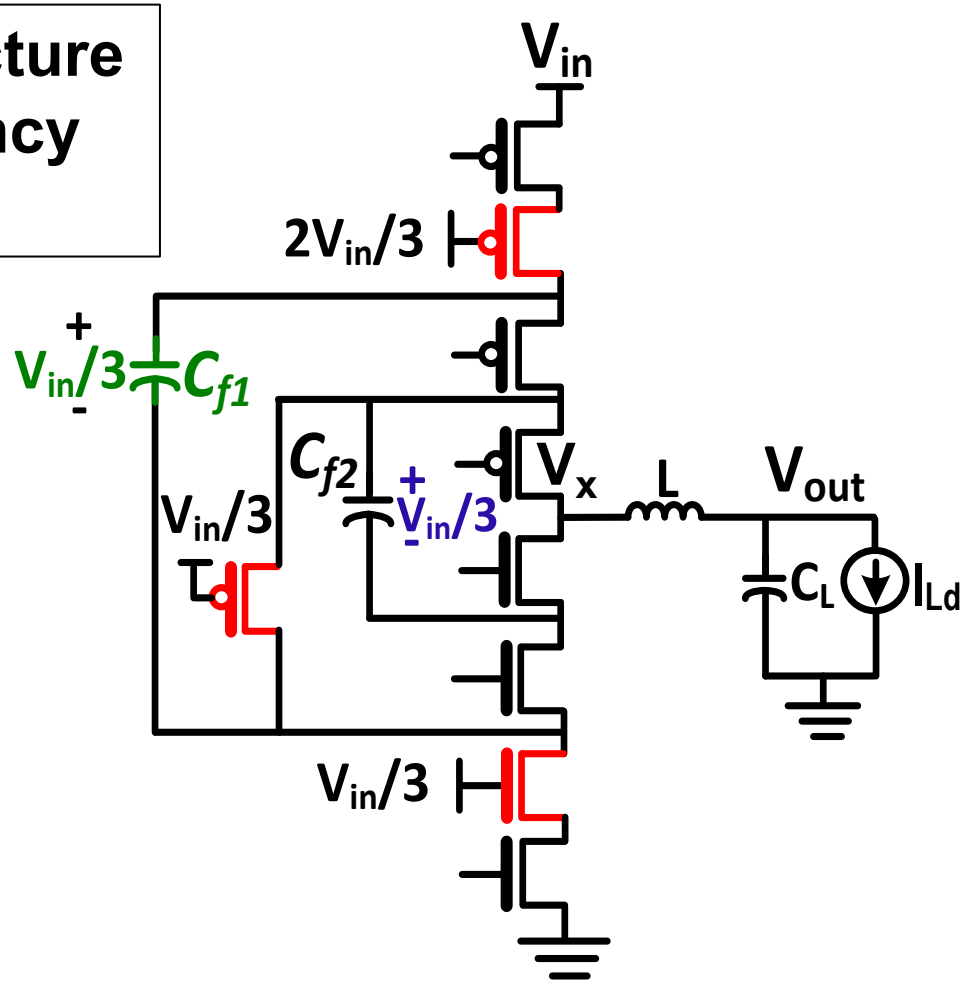



For same area, this topology can offer up to 12% higher efficiency

The overall efficiency is higher even with the added power switches because the proposed architecture allows larger passives for same area

# DCM-Operated Modified 4-Level Converter

**DCM-operated architecture to achieve high efficiency @ low load current**



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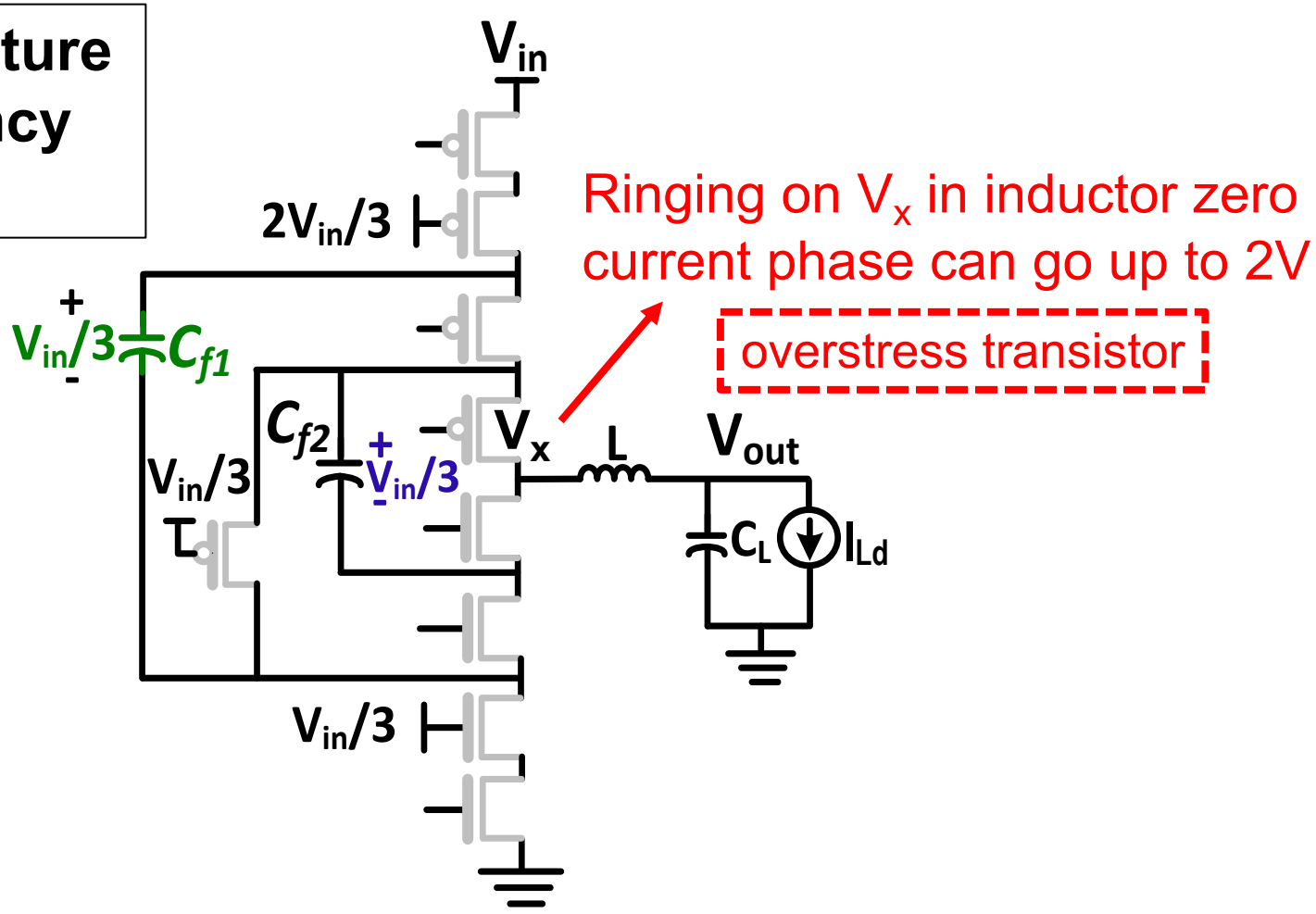

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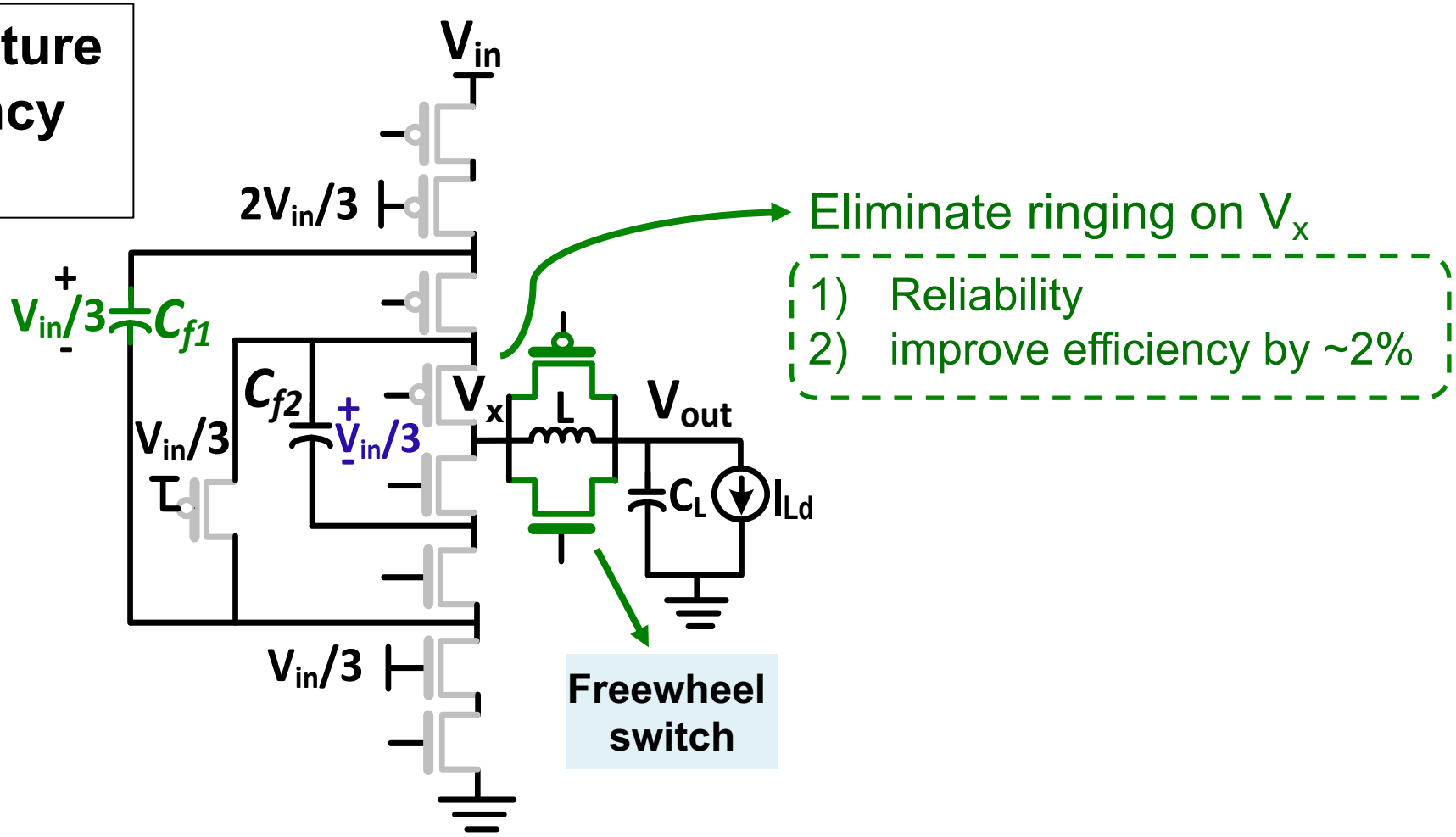


FW switches don't contribute to losses:

1) Turn ON only in zero current phase (~no conduction losses)
2) Sized much less than other FETs

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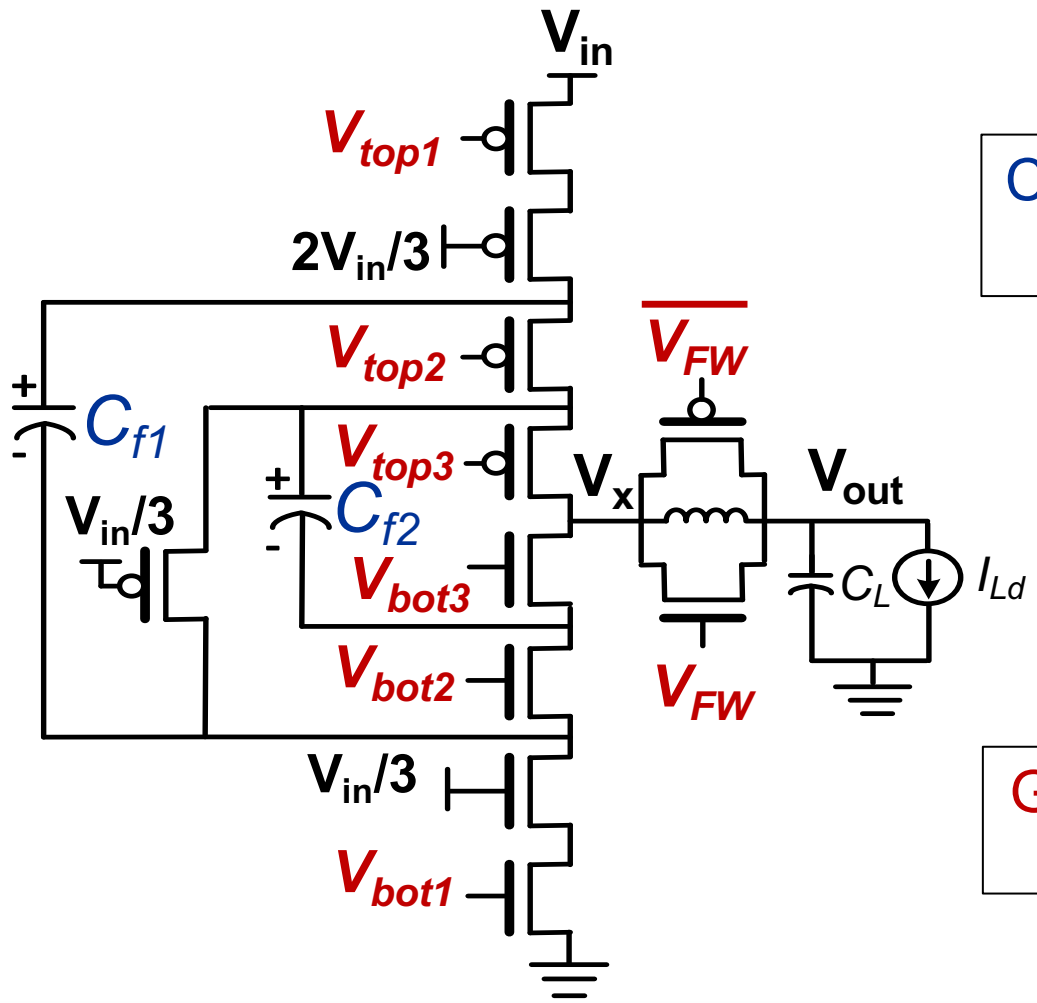
# Converter Switching Cycle: 7 Inductor Phases

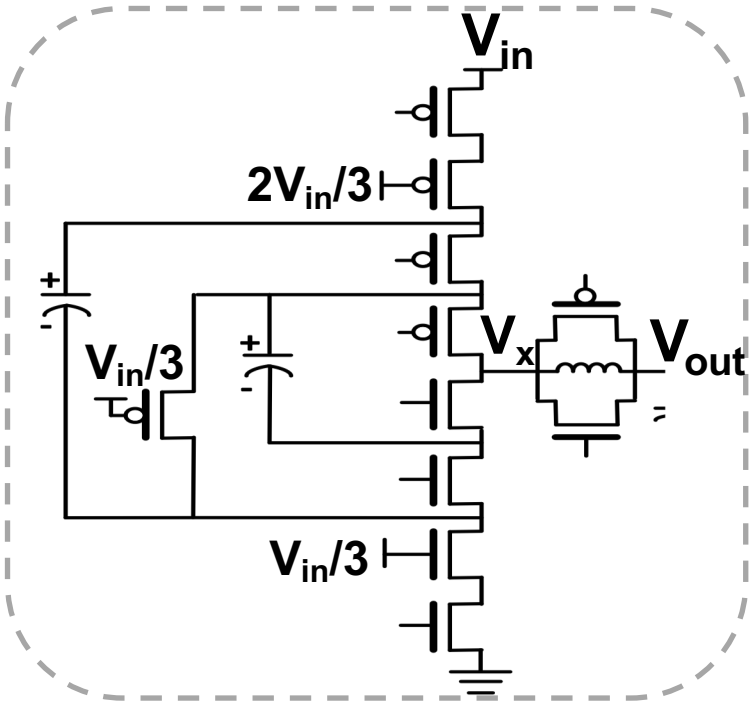



Capacitors steady state voltage:
$V_{f1} = V_{f2} = V_{in}/3$

Gate signals in each phase set such that no transistor exceeds $V_{in}/3$

There are 7 different inductor switching phases in one converter switching cycle

# Converter Switching Cycle (*7-phases*)

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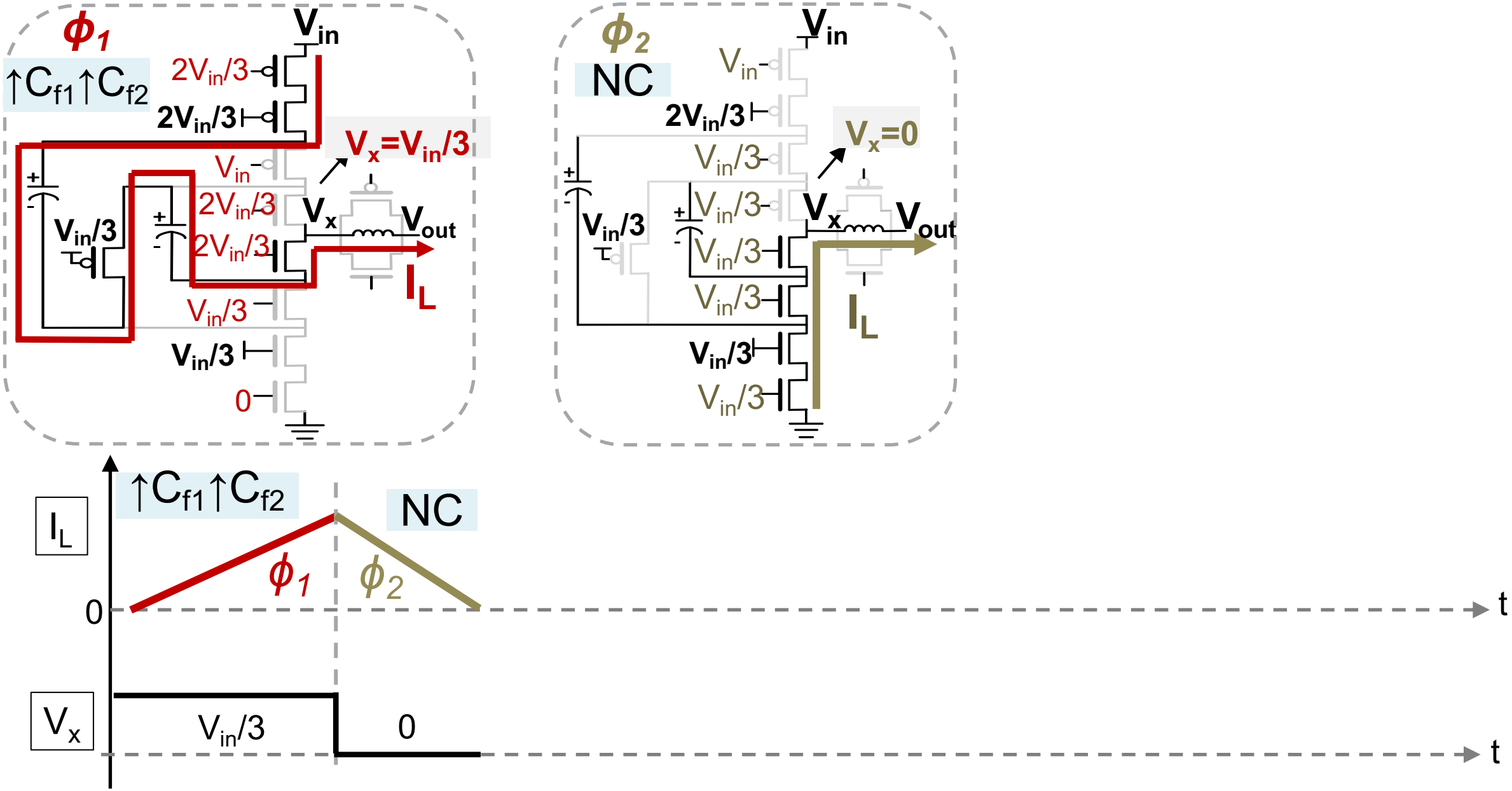

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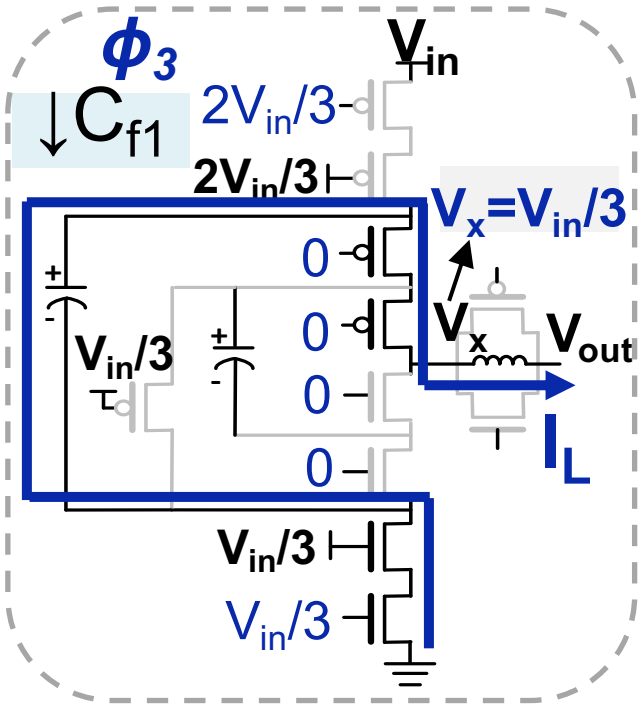


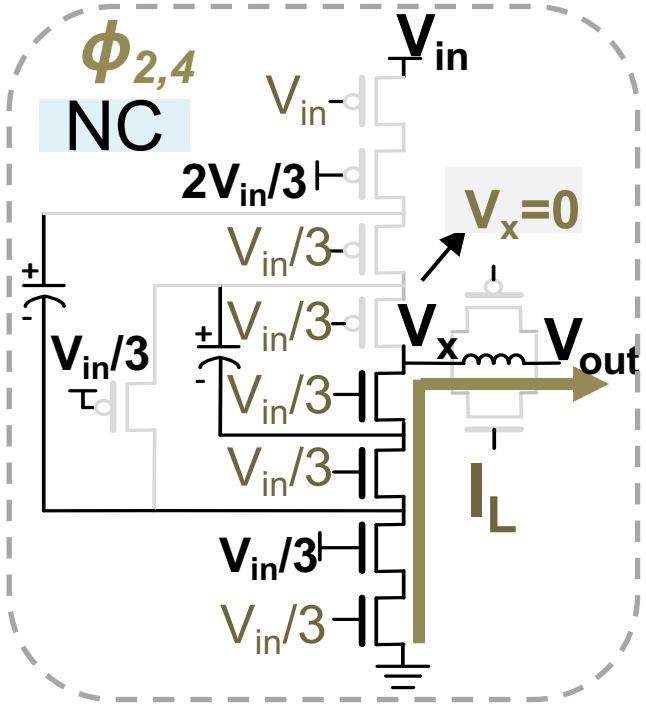


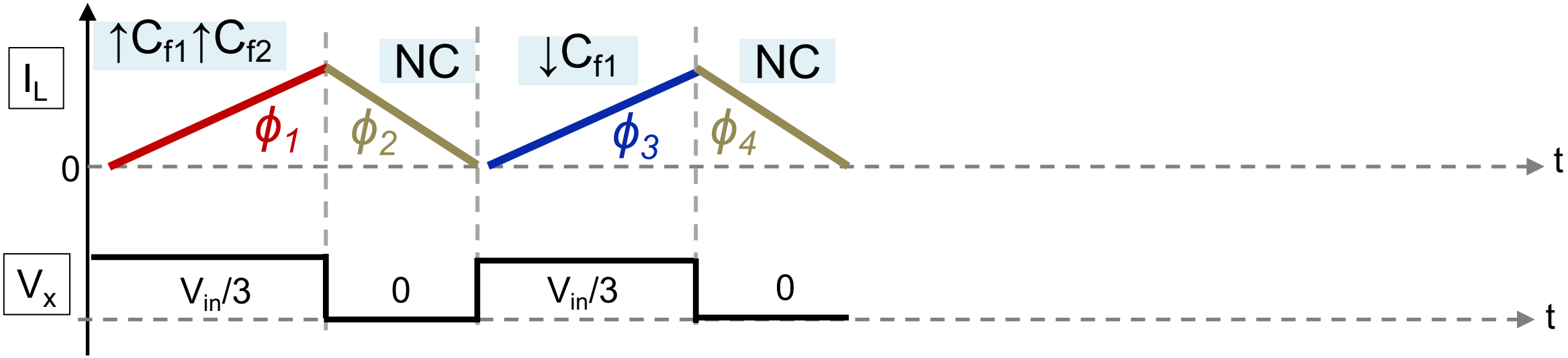

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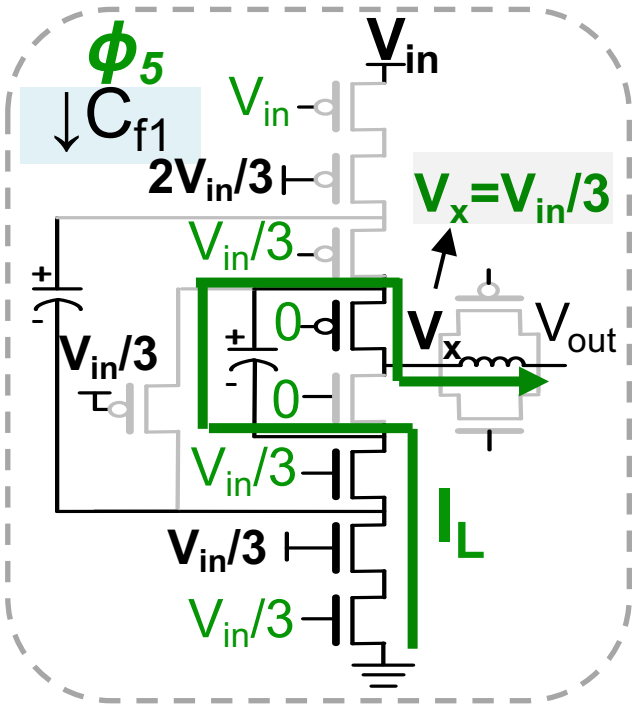


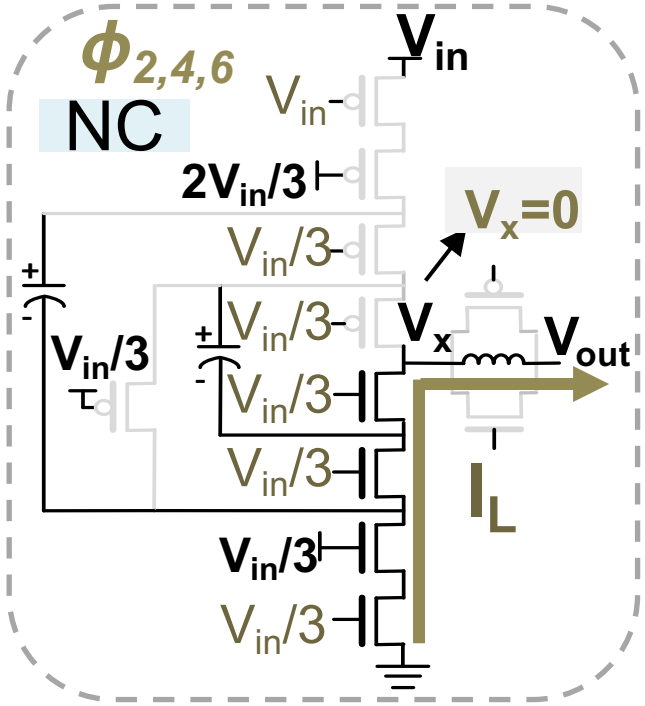


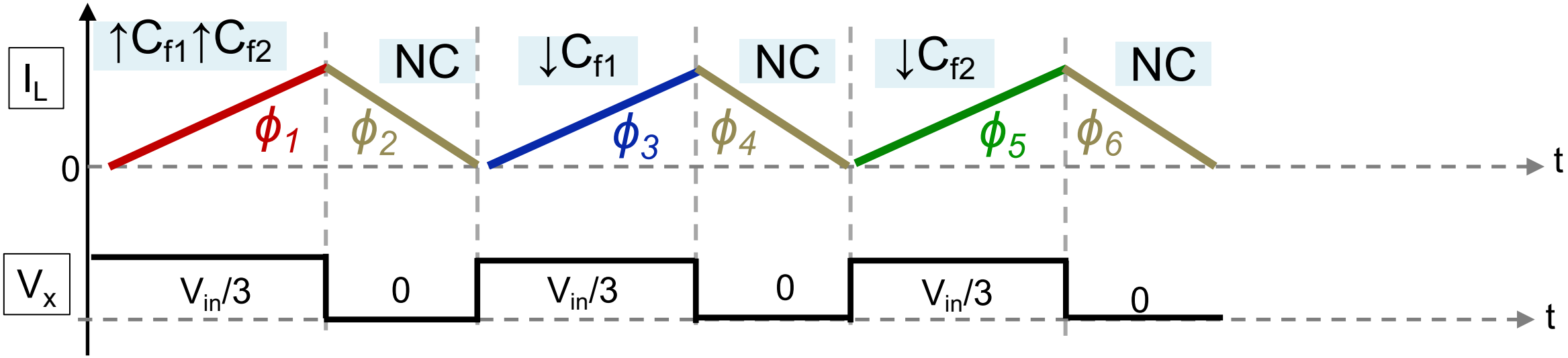

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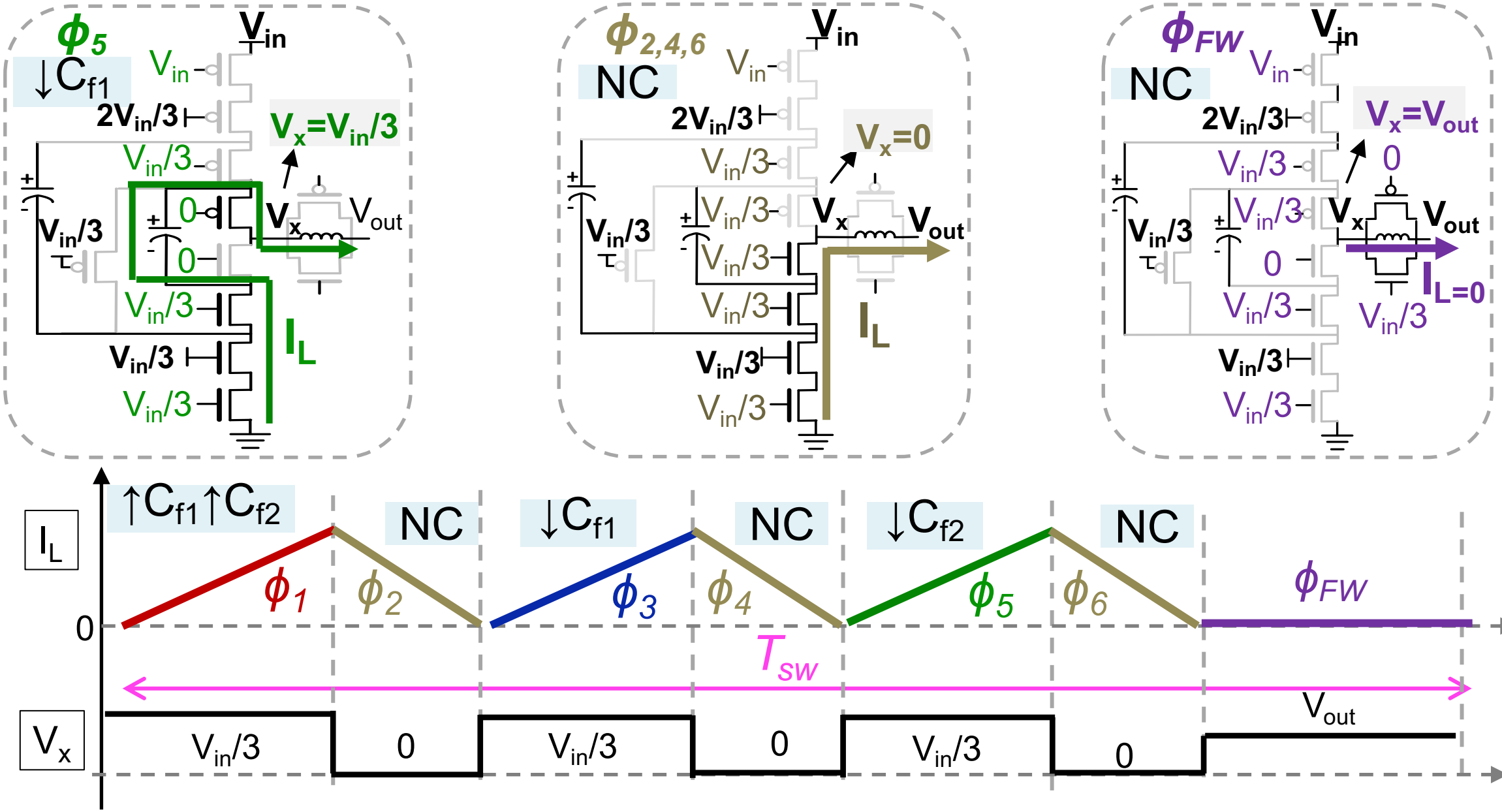
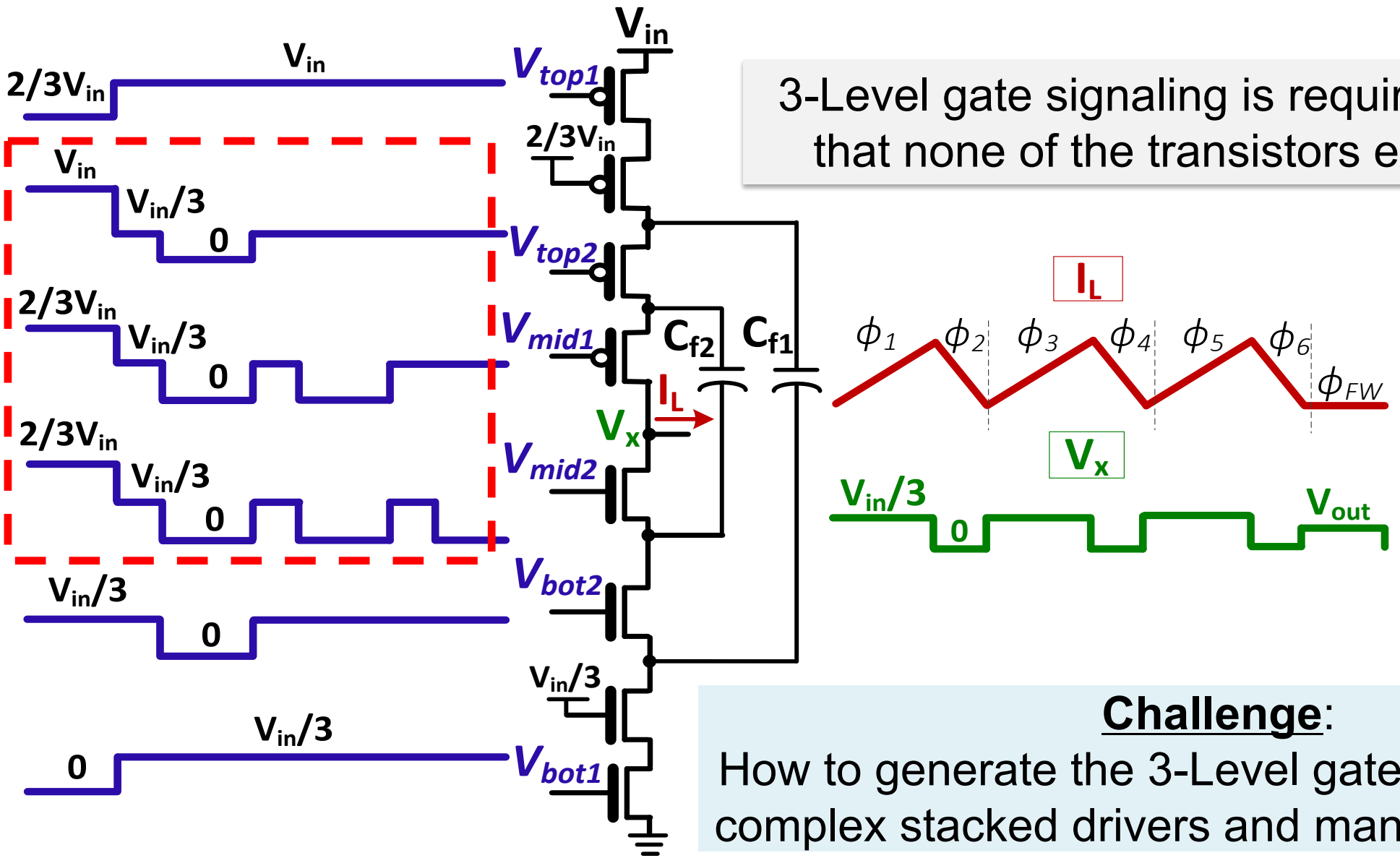


# Power Stage 3-Level Gate Signaling




3-Level gate signaling is required to ensure that none of the transistors exceed $V_{in}/3$




**Challenge**:

How to generate the 3-Level gate signals without complex stacked drivers and many level shifters?

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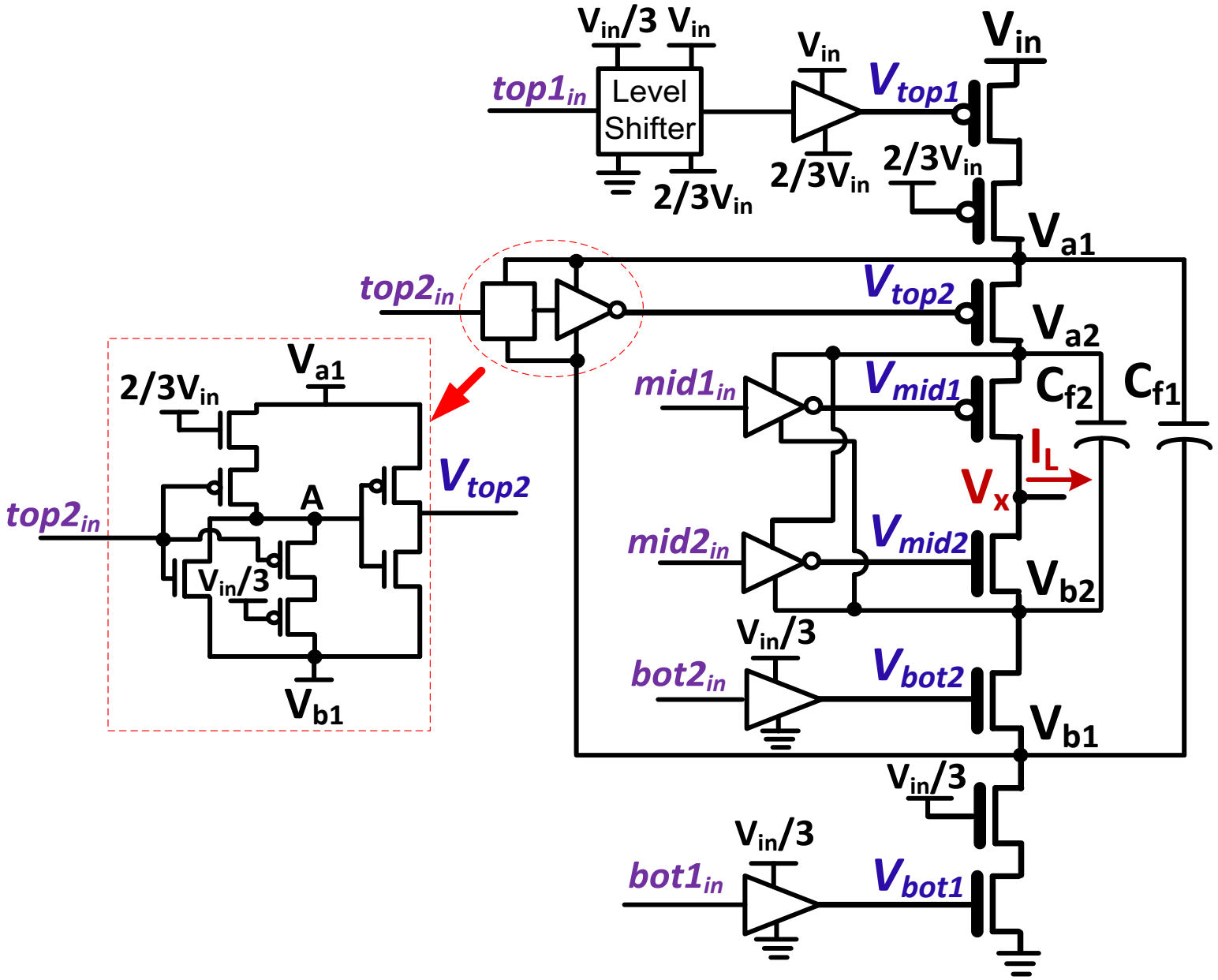
# Driver Architecture



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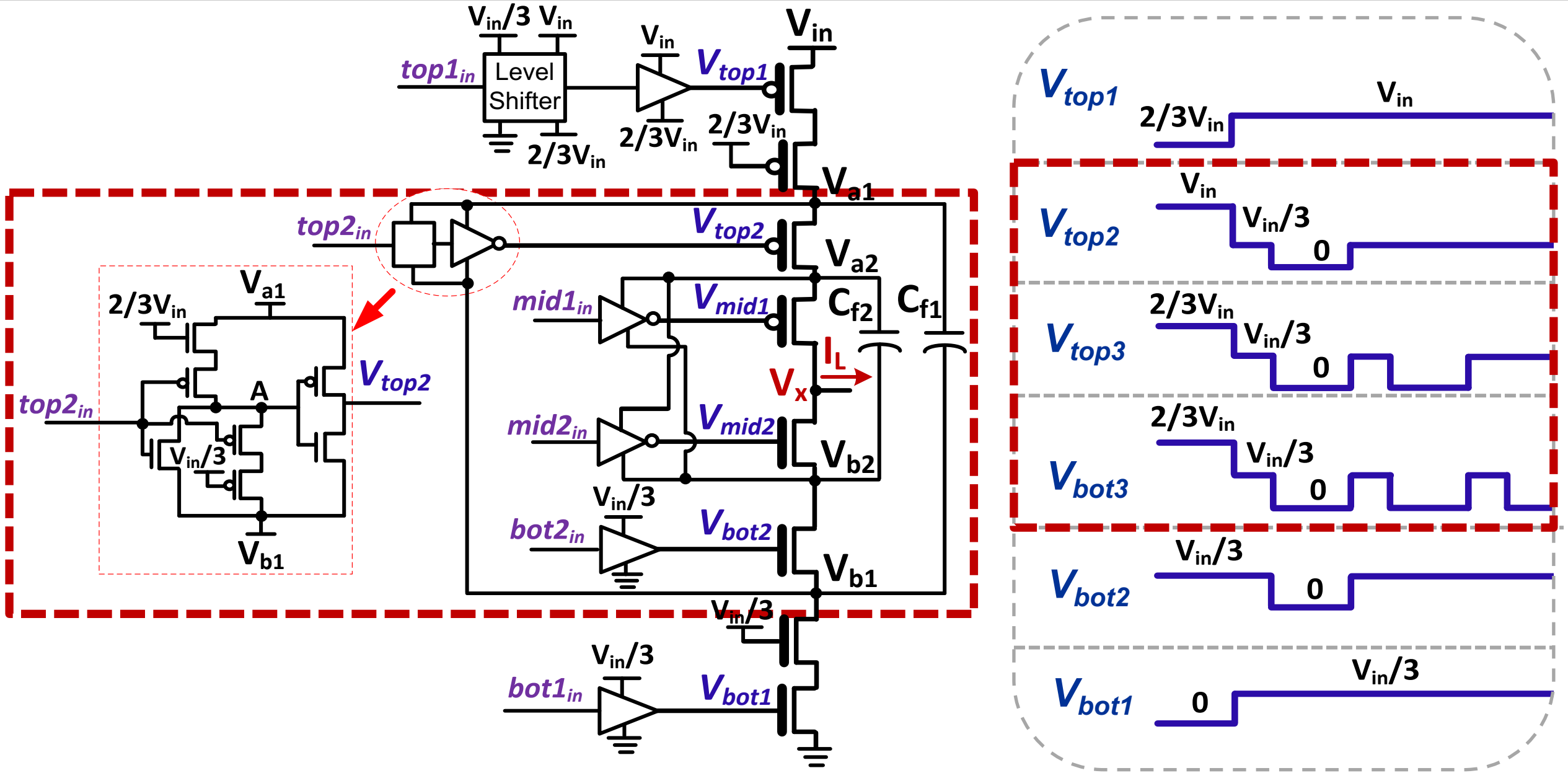
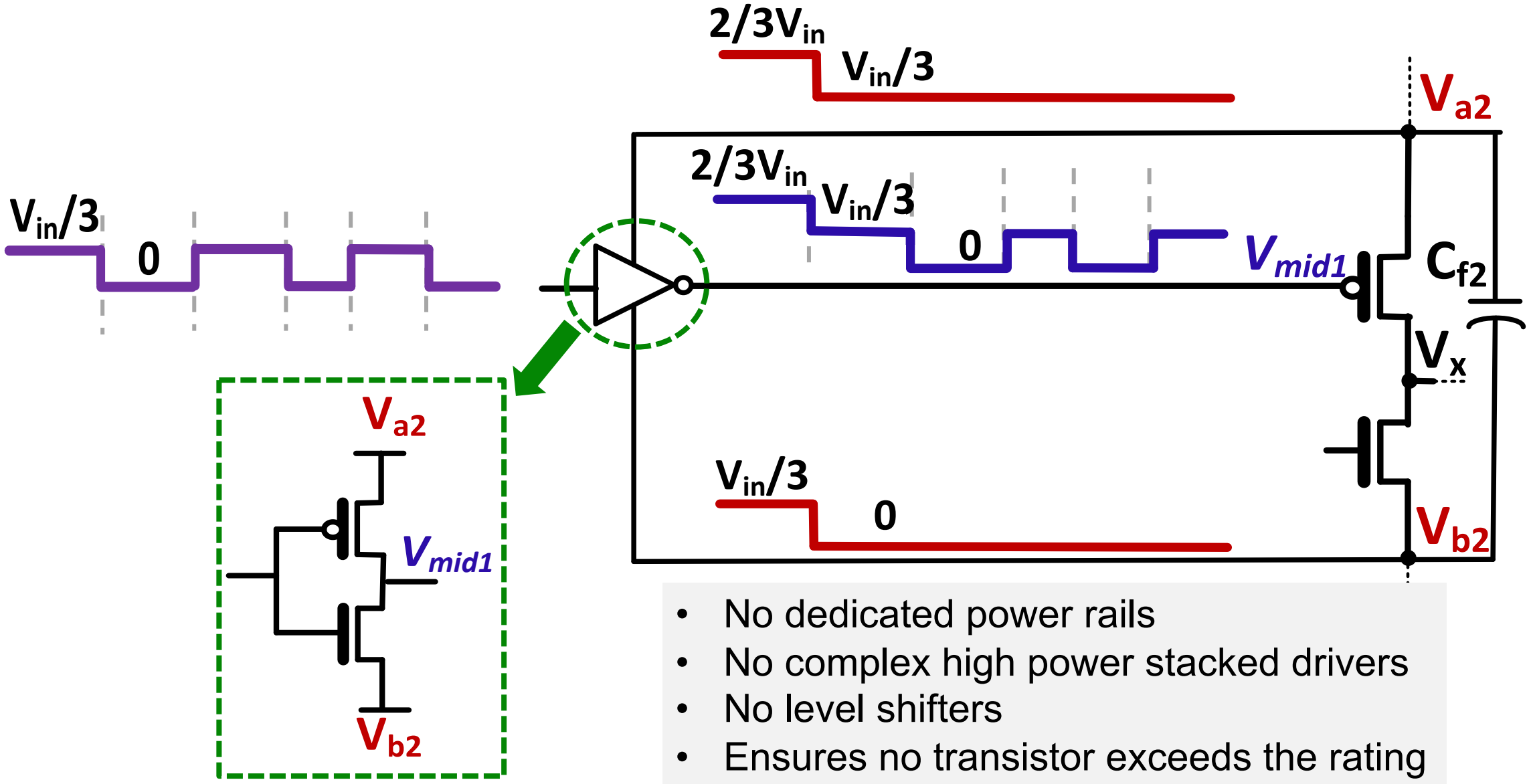
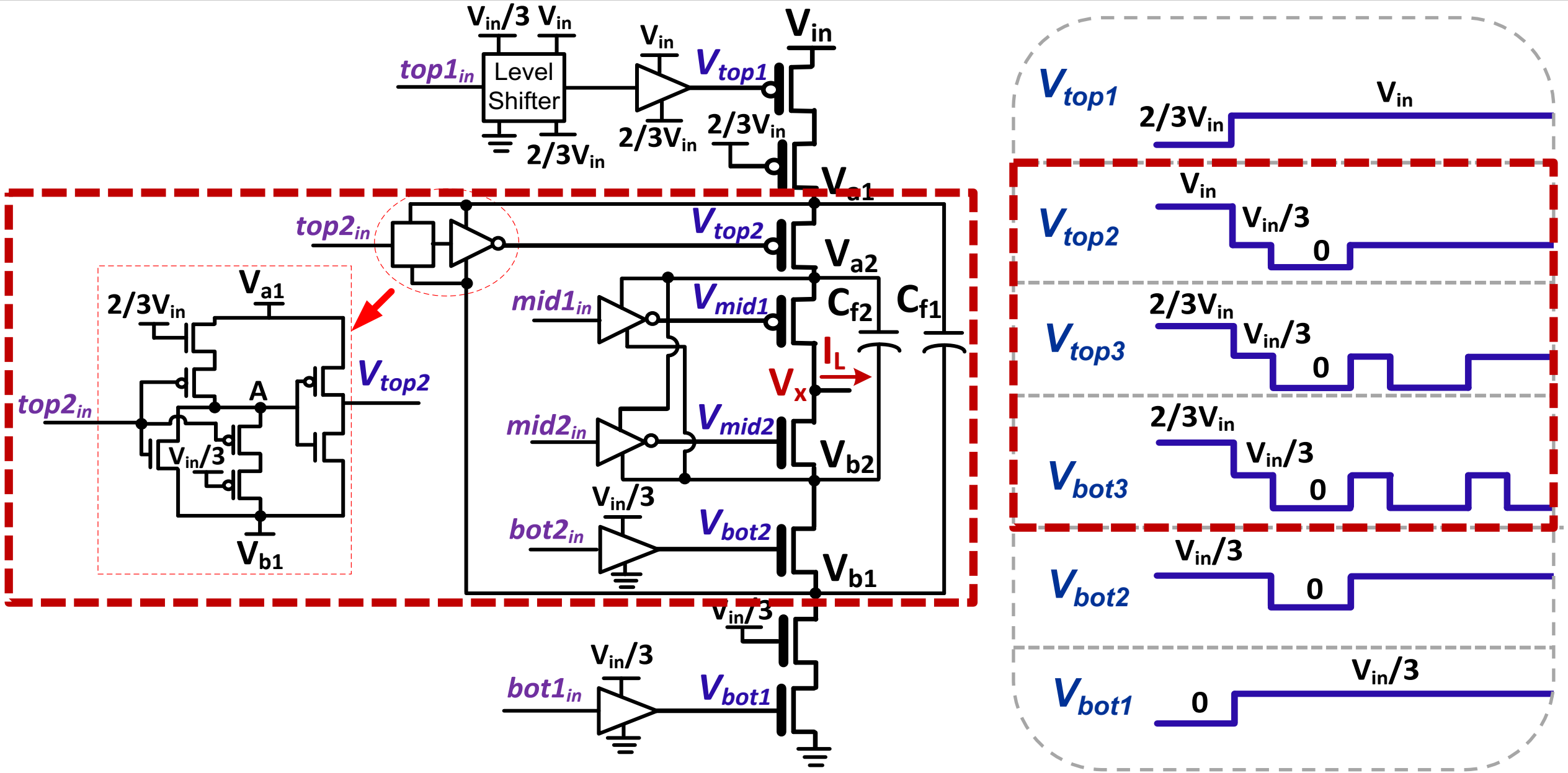


# 3-Level Gate Signaling Drivers




- No dedicated power rails
- No complex high power stacked drivers
- No level shifters
- Ensures no transistor exceeds the rating

# Driver Architecture



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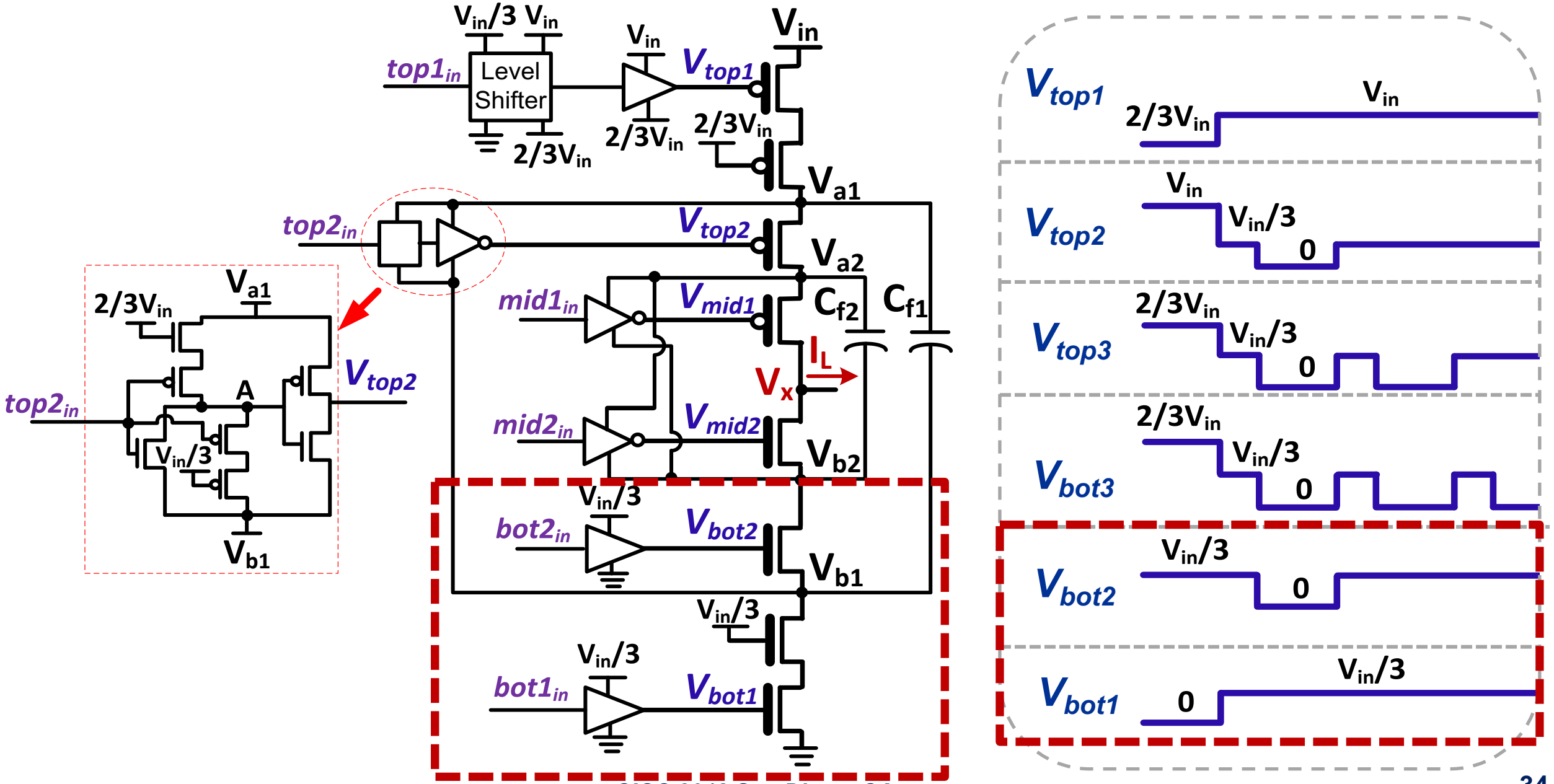

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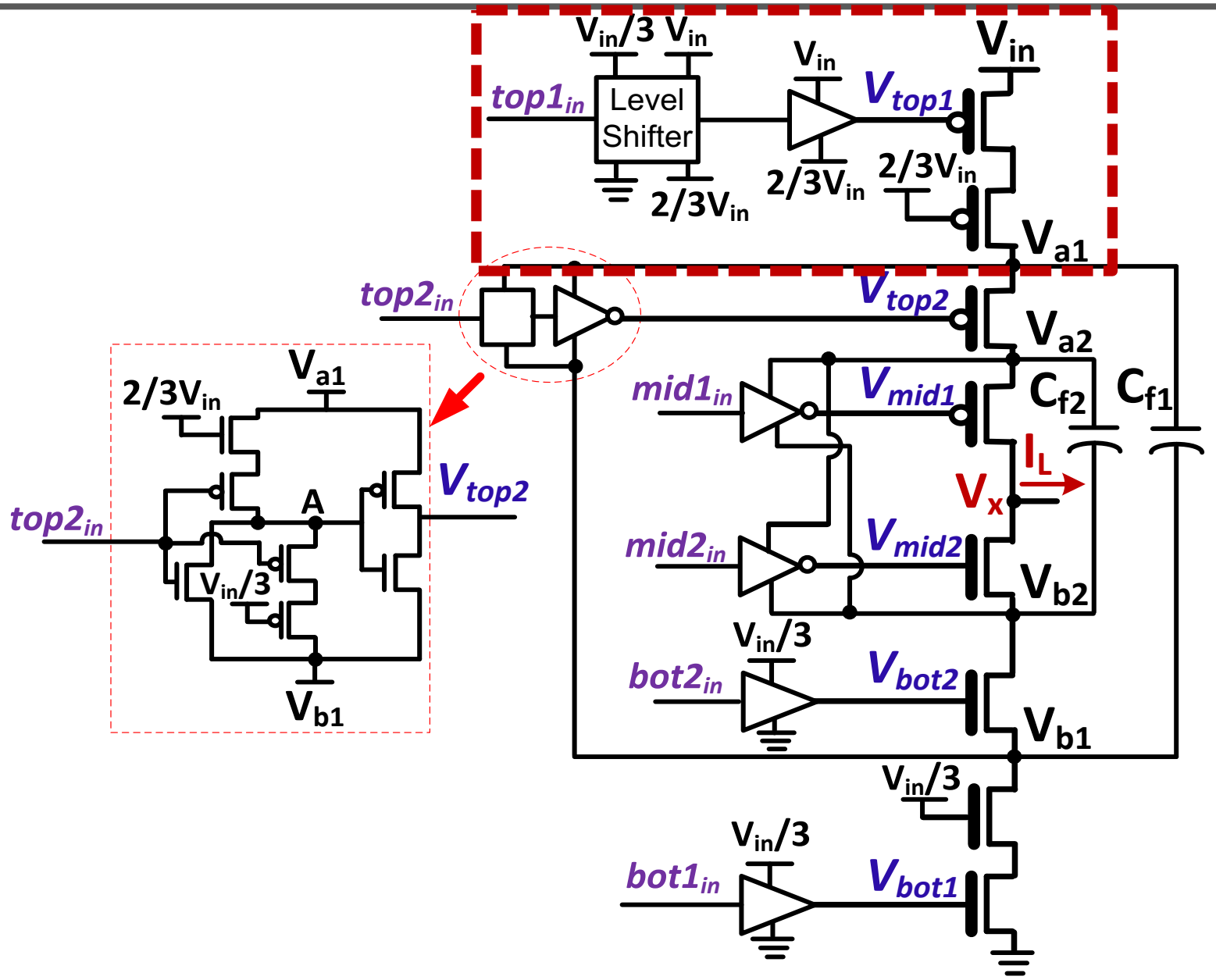
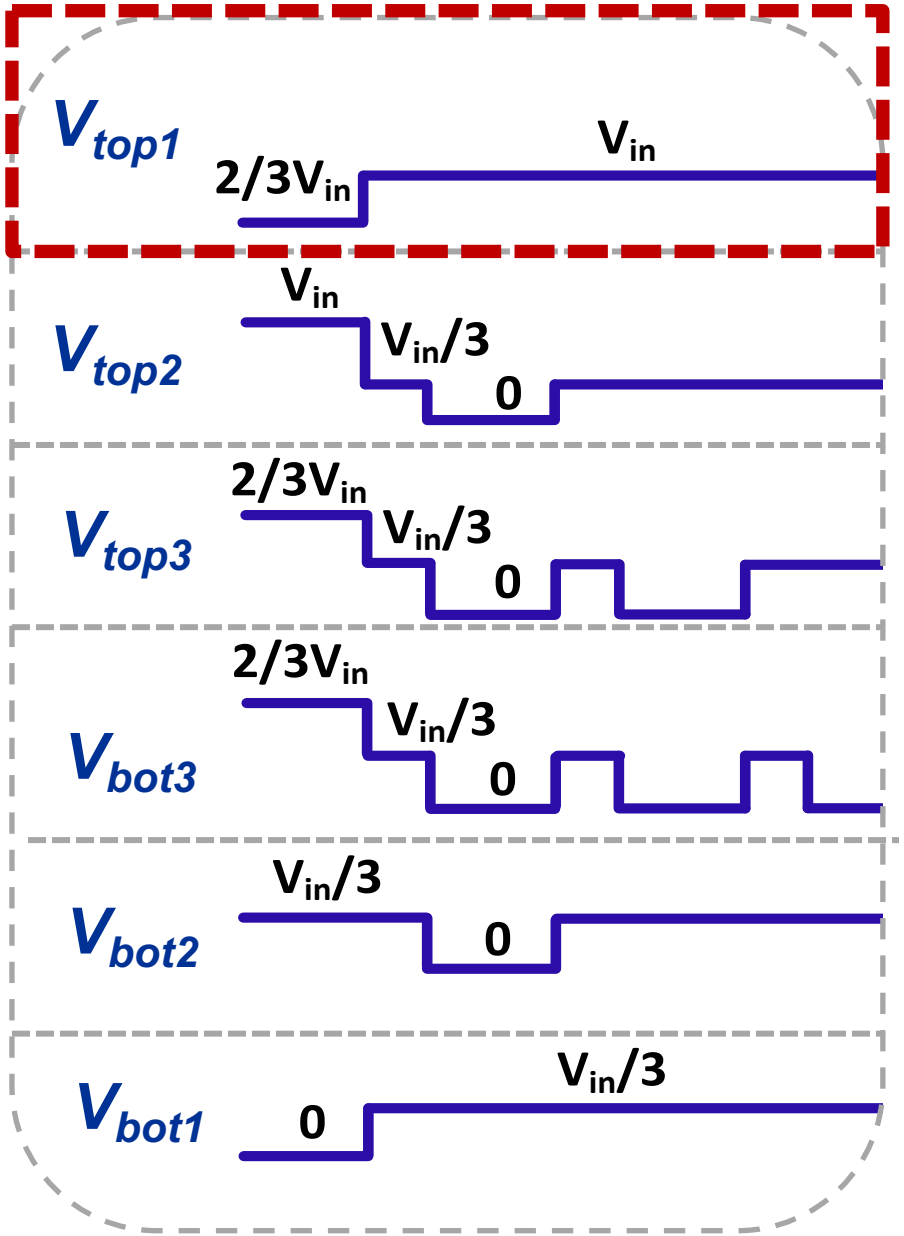


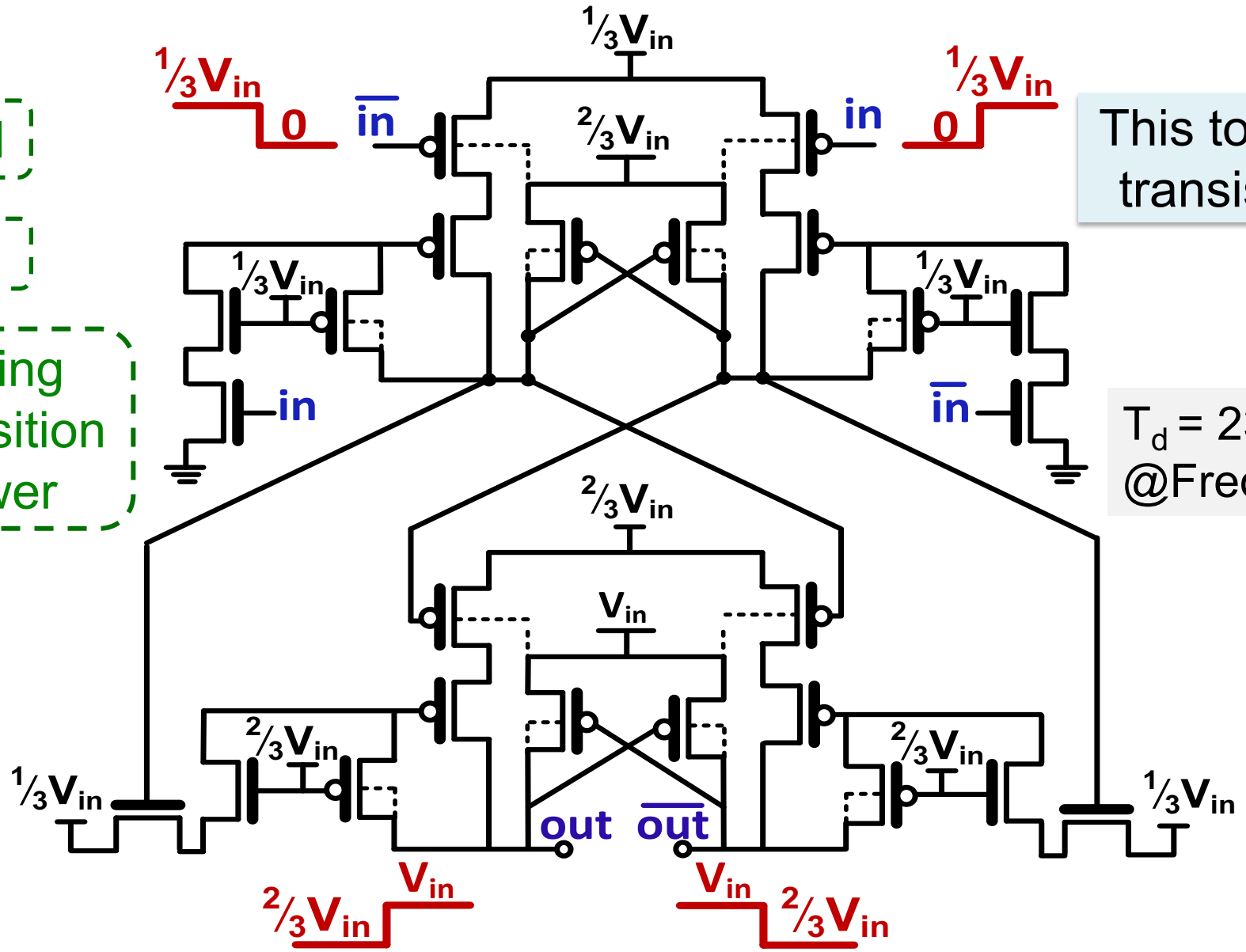



# New Level-Shifter Topology (0:$V_{in}$/3 → 2$V_{in}$/3:$V_{in}$)

All digital

No caps

Body biasing for fast transition & low power




This topology ensures no transistor exceeds $V_{in}$/3

$T_d$ = 230ps & P=1.27nW @Freq=1kHz &Vin=4.2V

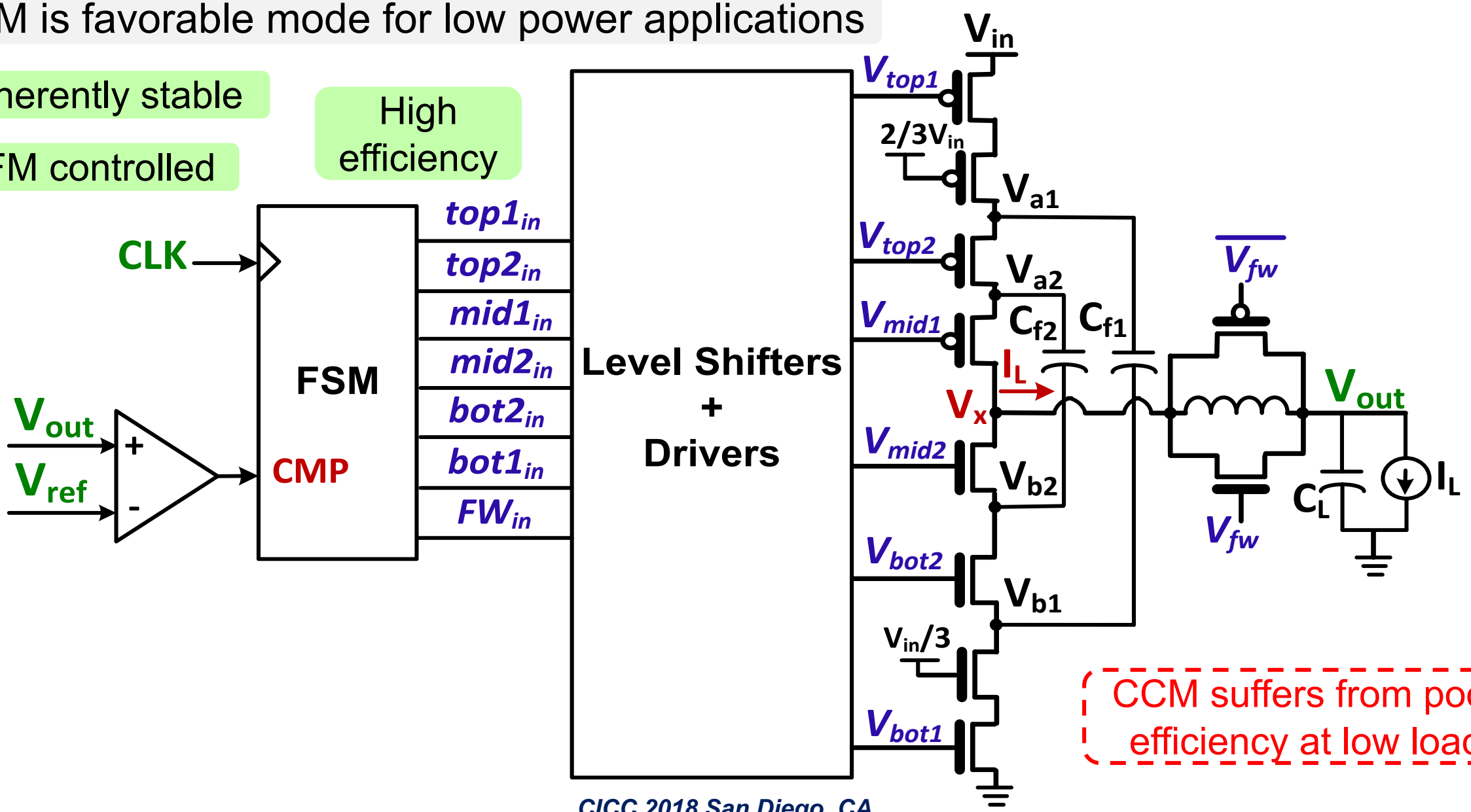
# DCM-Operated Top-Level Architecture

DCM is favorable mode for low power applications

Inherently stable

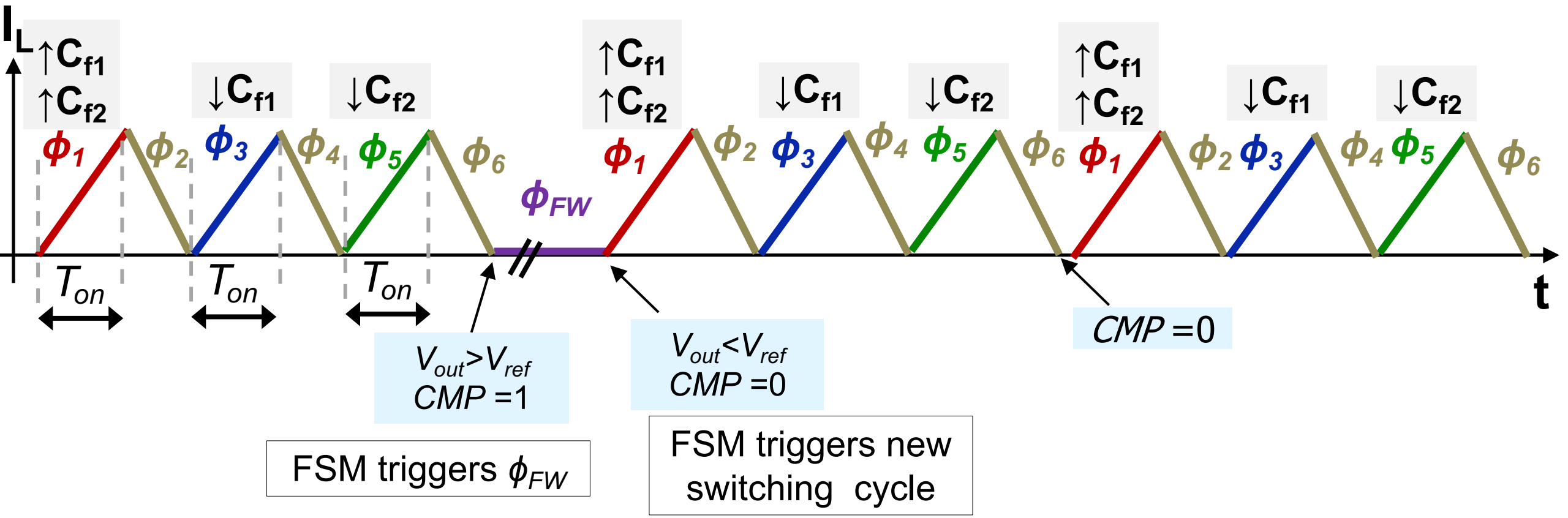
PFM controlled

High efficiency




CCM suffers from poor efficiency at low load

# Constant On-Time PFM Control




FSM checks the comparator output only at the end of $\phi_6$

- Not to interrupt the flying cap charge balance
- Reduce $F_{sw}$

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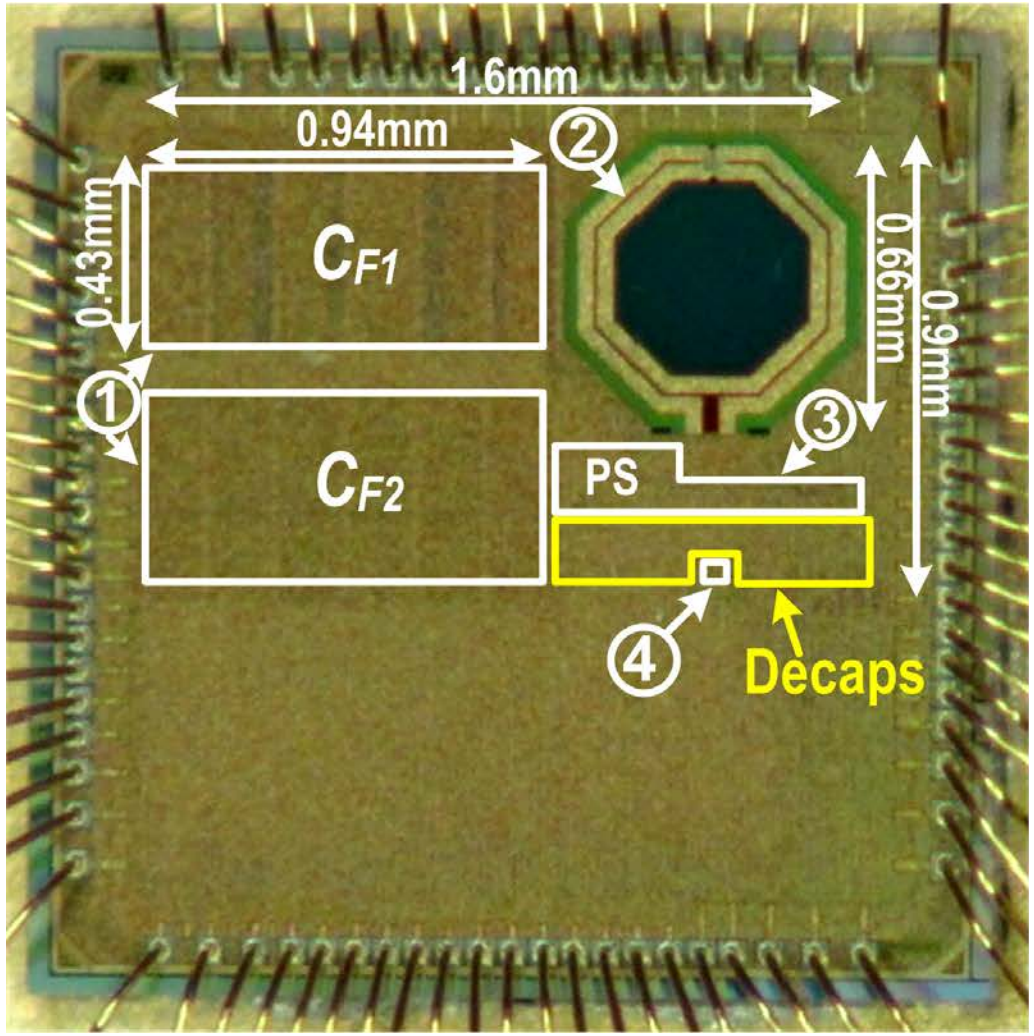
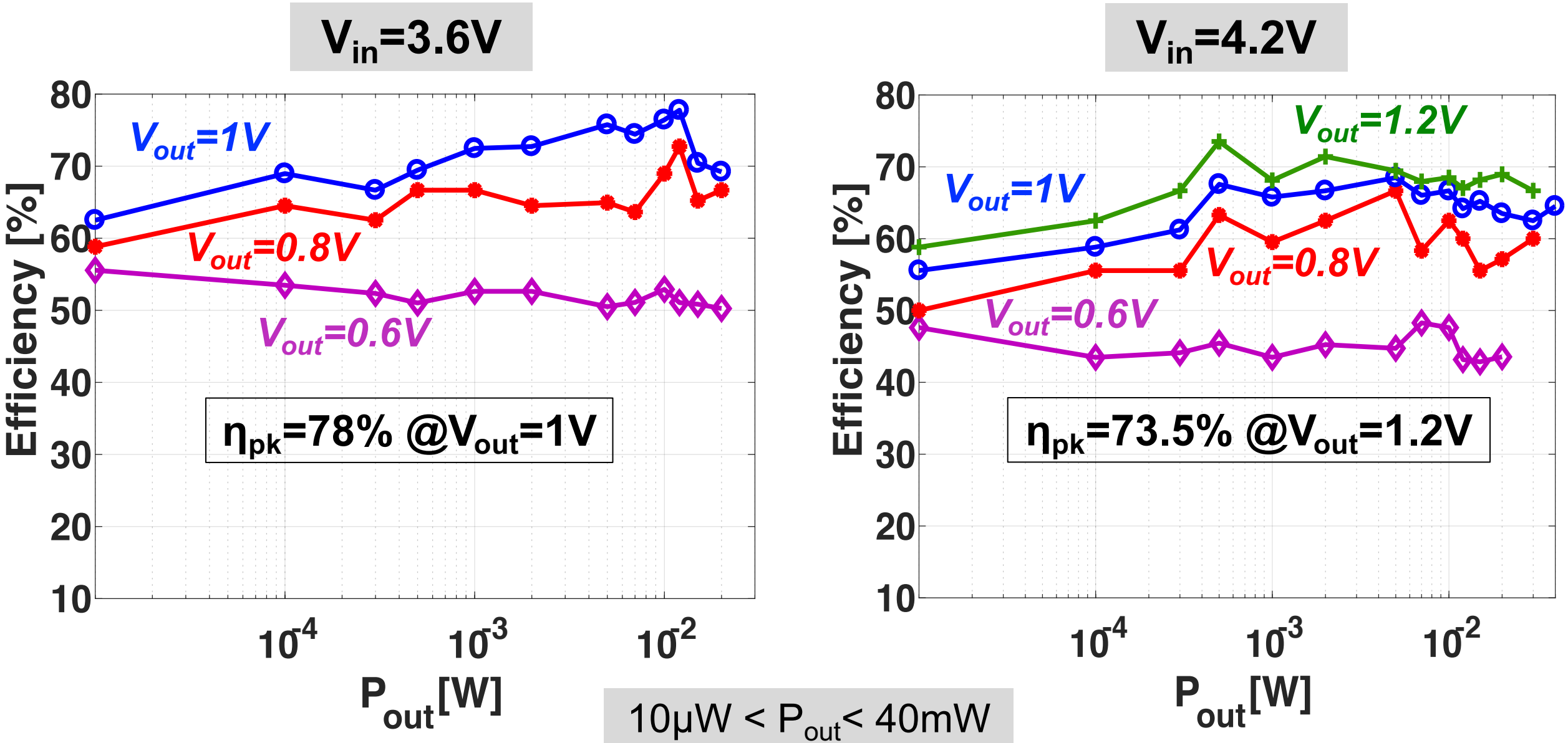
# Chip Microphotograph




1. Flying caps ($C_{f1}$=$C_{f2}$=5nF) [0.8084mm$^2$]
2. Inductor (*L=3nH, DCR=200mΩ*) [0.4356mm$^2$]
3. Power stage & drivers [0.06mm$^2$]
4. Digital controller [0.000225mm$^2$]

Implemented in 10-ML 28nm FDSOI
Total Area = 1.5mm$^2$

# Efficiency Measurement



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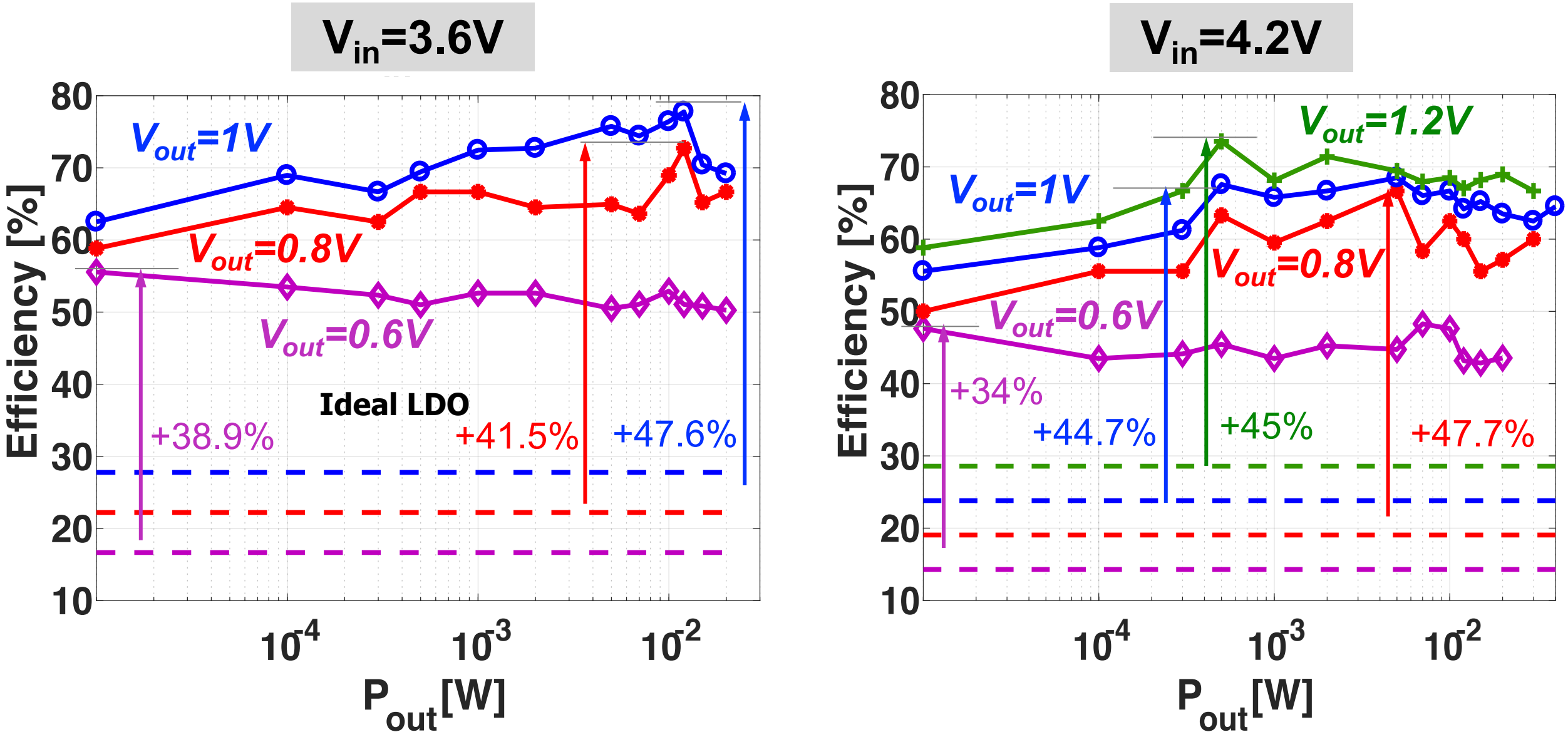
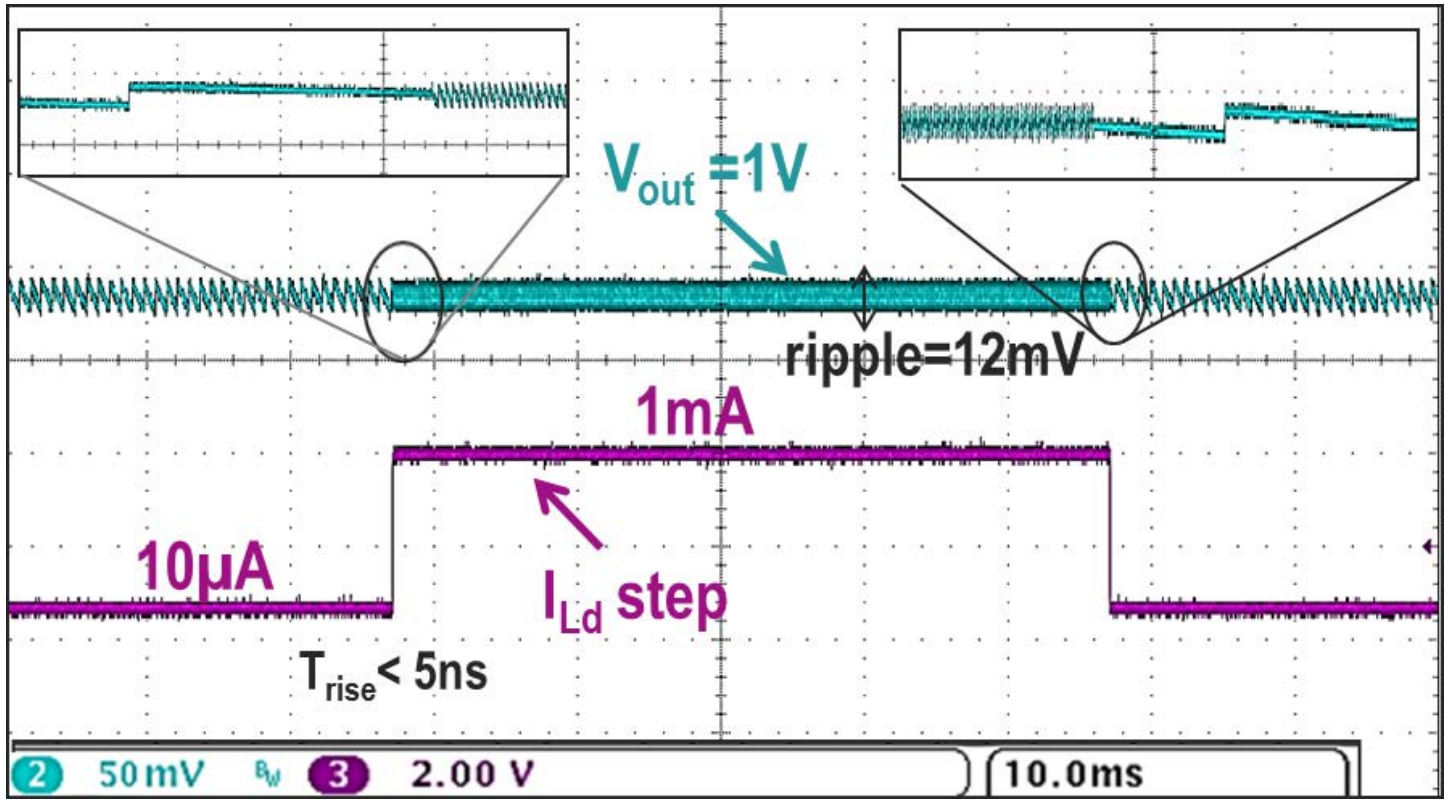


# Measured Load Step Response




Load step (10µA → 1mA) demonstrates:

- PFM control
- Negligible droop and output ripple=12mV

# Comparison with Prior State-of-Art

| | Breussegem, JSSC'11 | Le, ISSCC'13 | Bang, JSSC'16 | Kim, JSSC'12 | This Work |
|---|---|---|---|---|---|
| **Technology** | 90nm | 65nm | 180nm | 130nm | **28nm FDSOI** |
| **Li-ion Capability** | YES | YES | YES | NO | **YES** |
| **Topology** | SC | SC | SC | 3-Level | 4-Level |
| **L (H) / No of phases** | NA | NA | NA | 4n / 4 phases | 3n / 1 phase |
| **CR** | 1/2 | 1/3, 2/5 | 117 CRs | NA | NA |
| **$V_{in}$ (V)** | 3-3.9 | 3-4 | 3.4-4.3 | 2.4 | **2.8 - 4.5** |
| **$V_{out}$ (V)** | 1.3@Vin=3<br>1.42@Vin=3.3<br>1.5@Vin=3.6 | 1 | 0.45-1.5 | 0.4-1.4 | 0.6-1.2 |
| **$F_{max}$ (MHz)** | 70 | 300 | 2.7 | 200 | 200 |
| **$P_{out}$ (mW)** | 1*-150 | 6*-162 | 0.001*-0.45 | 120*-1000 | 0.01-40 |
| **Dynamic Range ($P_{max}/P_{min}$)** | 150 | 27 | 450 | 8.3 | **4,000** |
| **Area ($mm^2$)** | 3.6* | 0.64 | 1.69 | 5 | 1.5 |
| **Overall peak efficiency @1/CR** | 77.3%@2.3 | 74.3%@3.6 | 72%@2.6 | 77%@2.2* | **78%@3.6** |
| **Maximum improvement over LDO@ $(1/CR)_{range}$** | 33.9%*<br>@2.3 | 35-45%*<br>@3-4 | 21%-49.5%*<br>@3-7 | 18-31%*<br>@2-4 | **34-50.5%<br>@3-7** |

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**PFM control**

$F_{sw\text{-}out} \leq 200MHz$

$1kHz \leq F_{sw\text{-}in} \leq 67MHz$

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# Outline

- Prior Work
- Proposed Hybrid Architecture
- Switching Phases of the Proposed Architecture
- Circuit Details
- Measurement Results
- Conclusion

# Conclusion

- This work demonstrated that integrating a DC-DC converter compatible with Li-ion battery voltage (2.8-4.2V), using low-voltage transistors (1.5V) in scaled CMOS is feasible.
- A modified 4-level topology was proposed to reduce the cap area by 4x
- The proposed architecture is DCM-operated to achieve high efficiency at a low load range appropriate for IoT applications (10μW-40mW)
- The proposed converter achieved a peak efficiency of 78% and 34%-50.5% efficiency improvement over an ideal LDO

The authors thank ST Microelectronics for chip fabrication