A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving 0.7W/mm^2 Power Density and 94% Peak Efficiency

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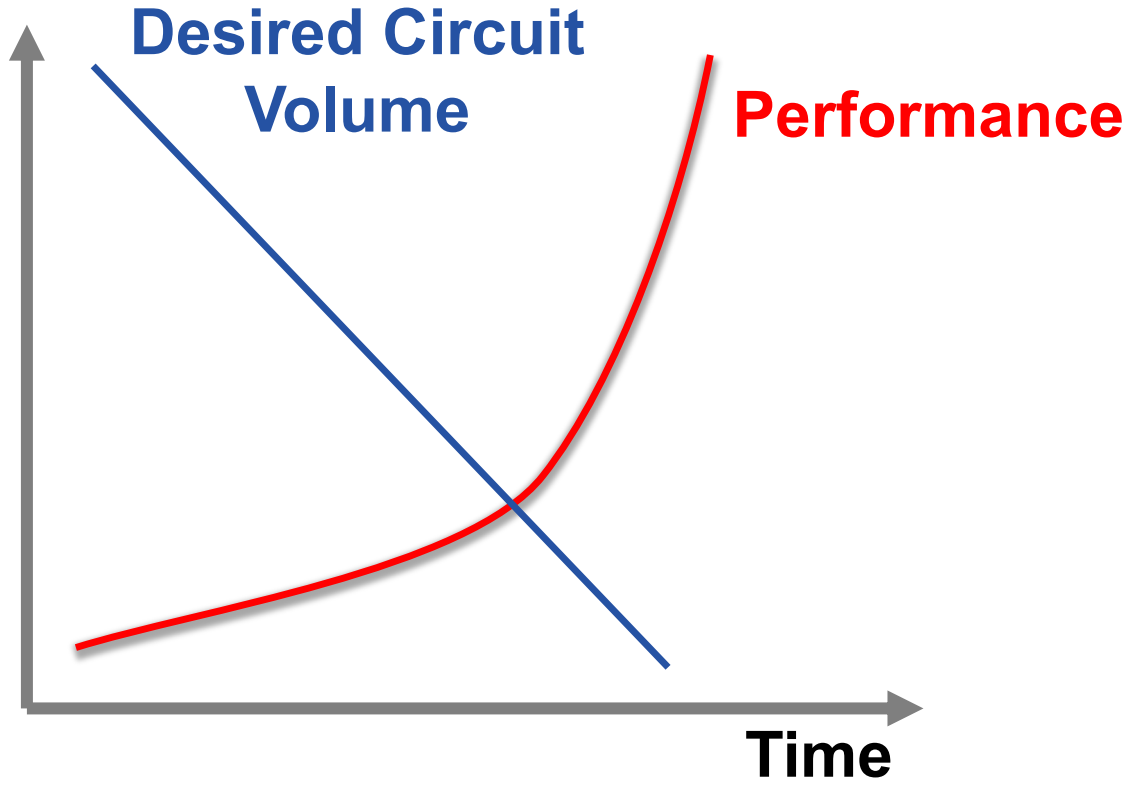
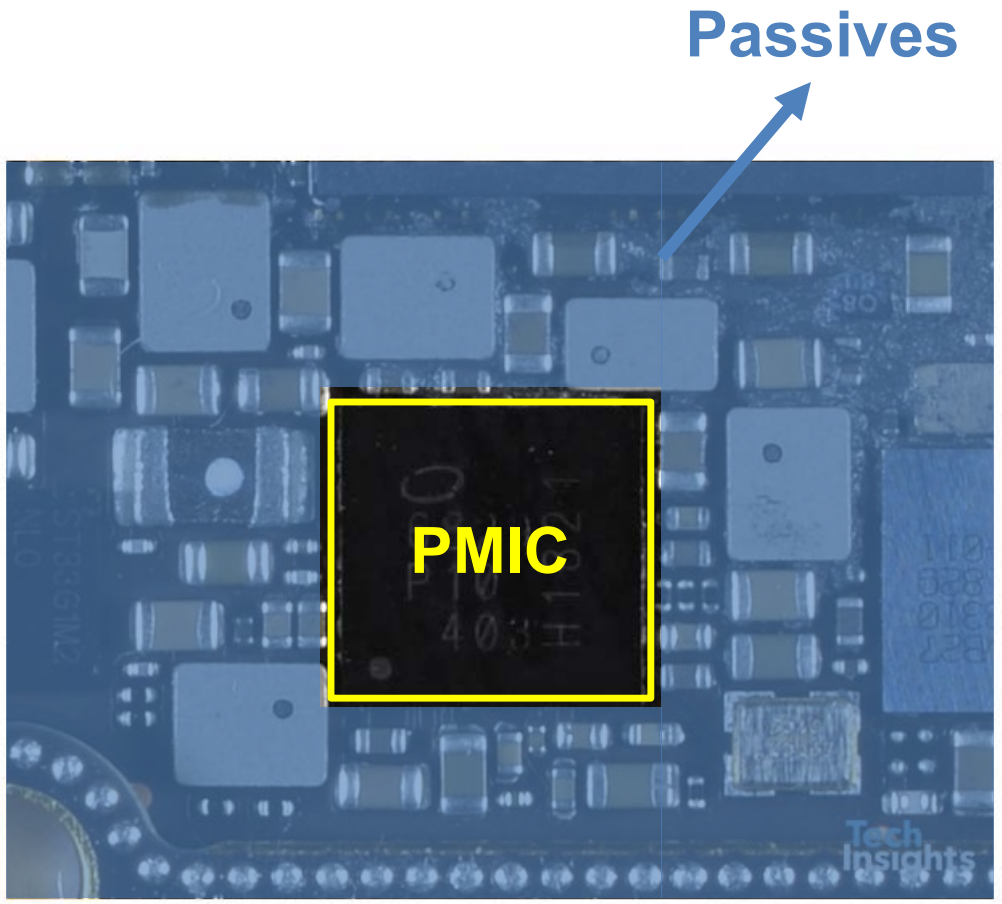
UC San Diego

Motivation

- Consumer electronics are shrinking down while performance demand is increasing:





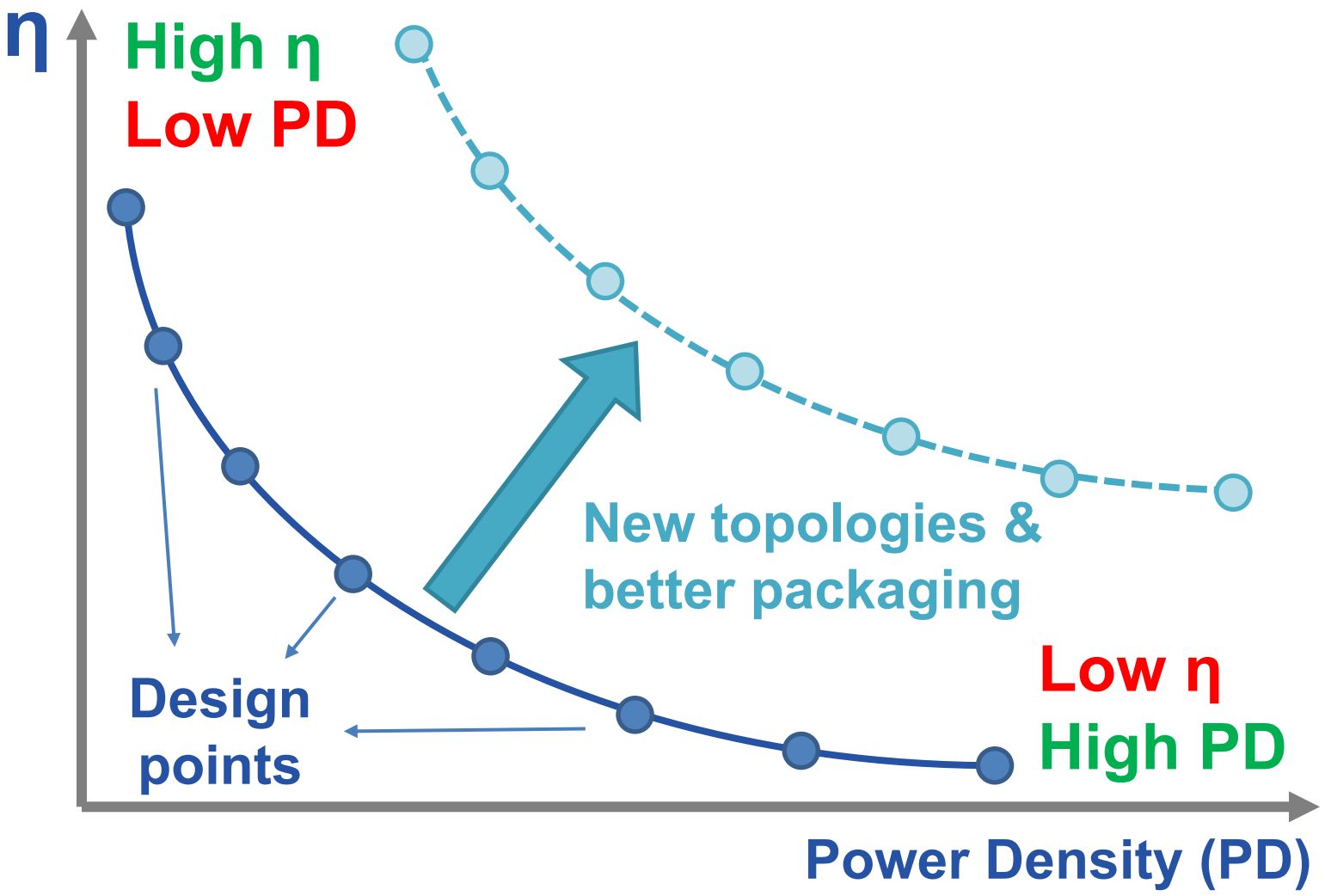
PCB of iPhone Xs Max*

*https://www.techinsights.com/

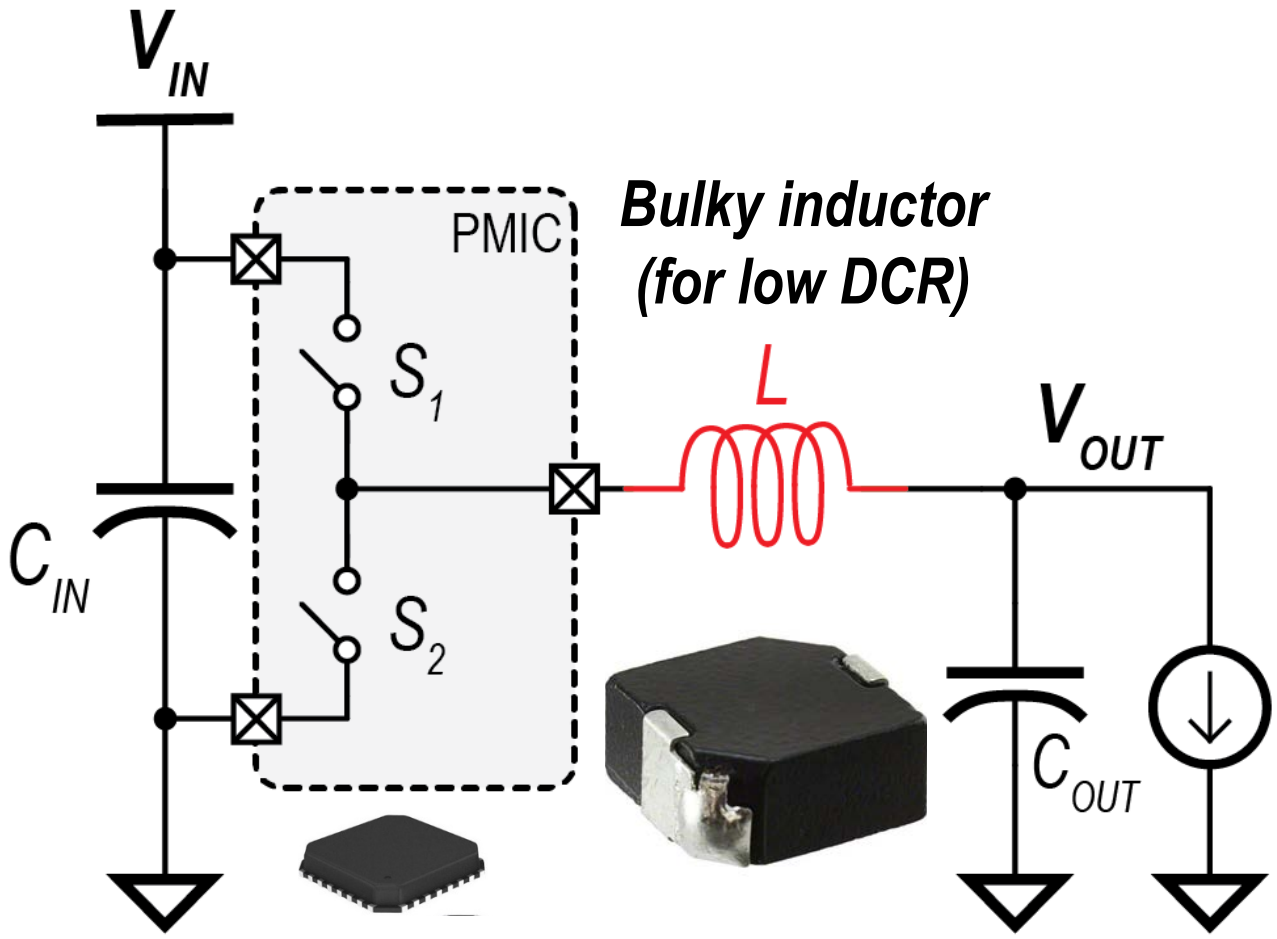
More power demand in a smaller area without sacrificing battery life

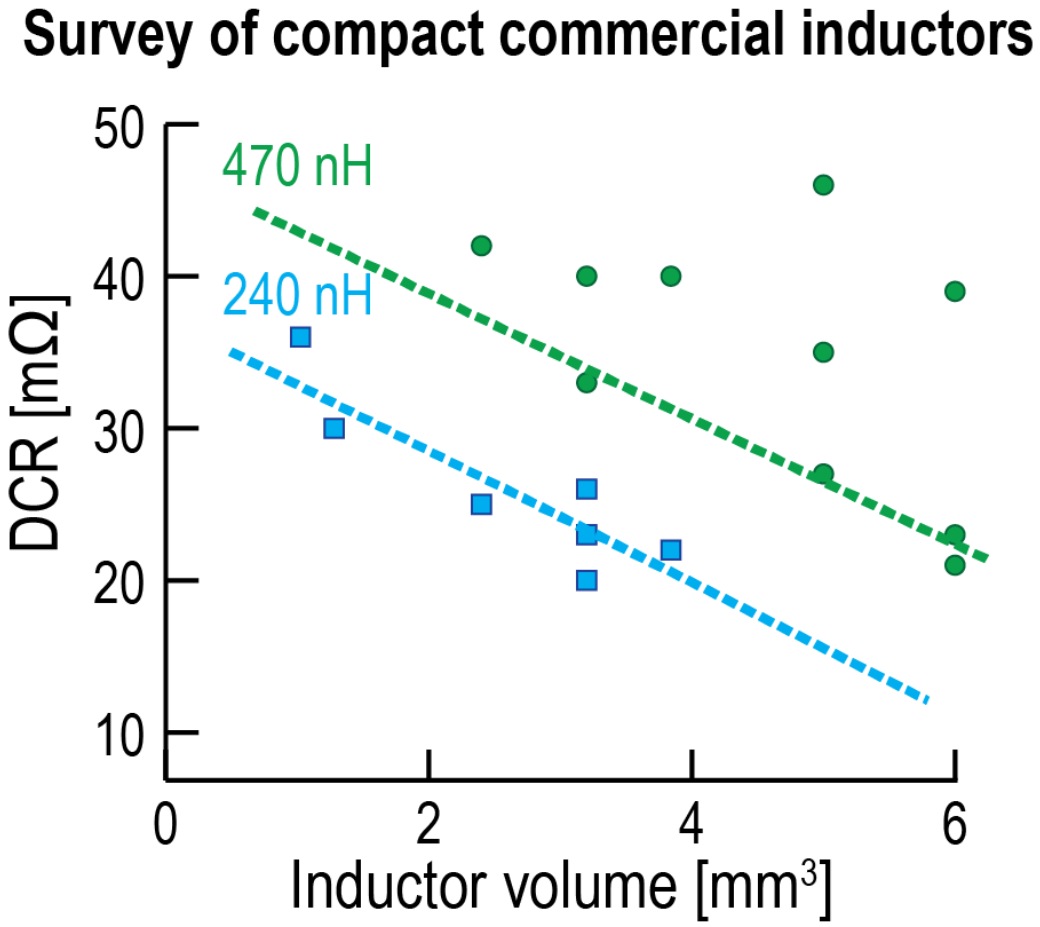
Motivation

- Tradeoff between efficiency and power density:



Conventional Buck Converter





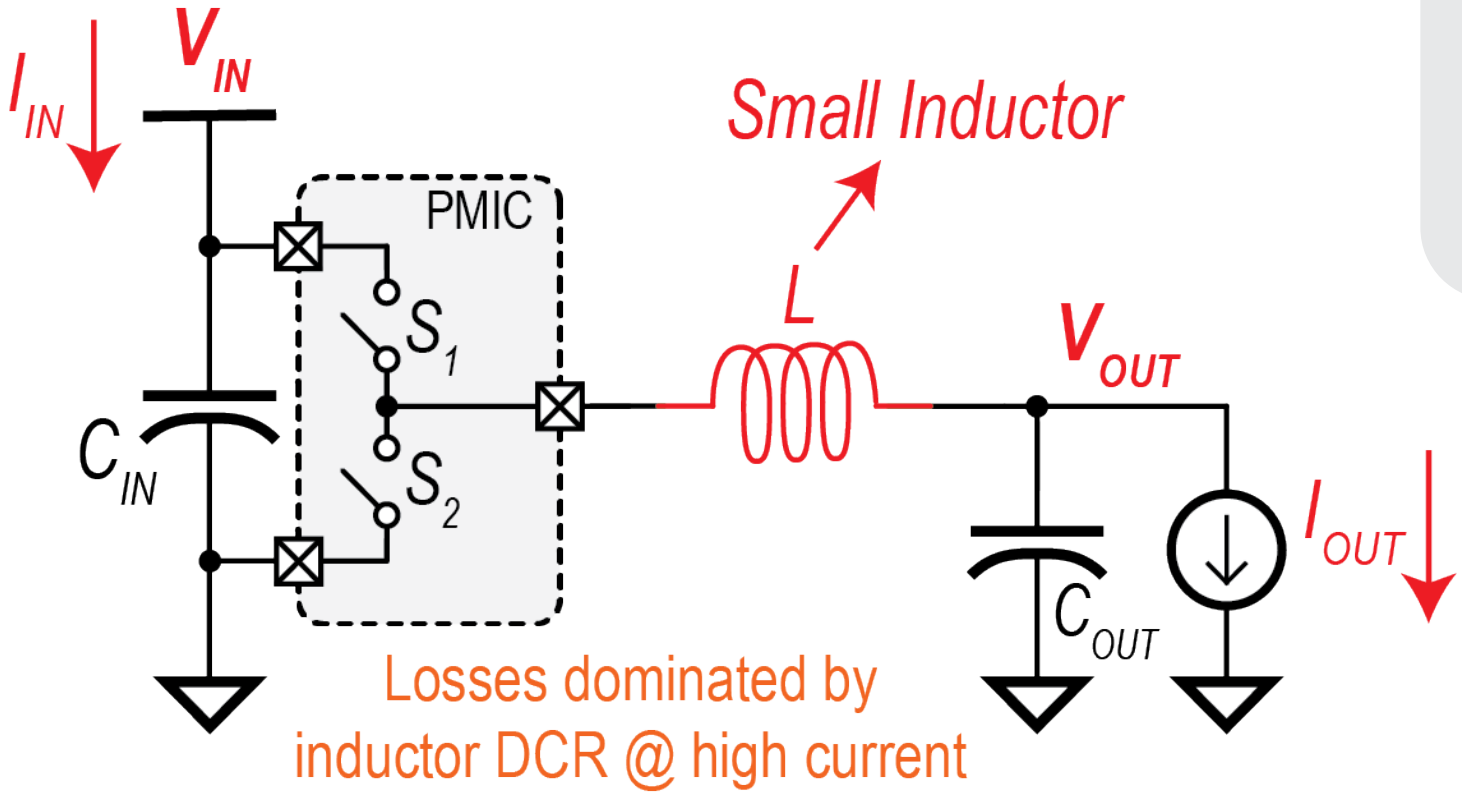
PMIC only:
PD > 1W/mm²

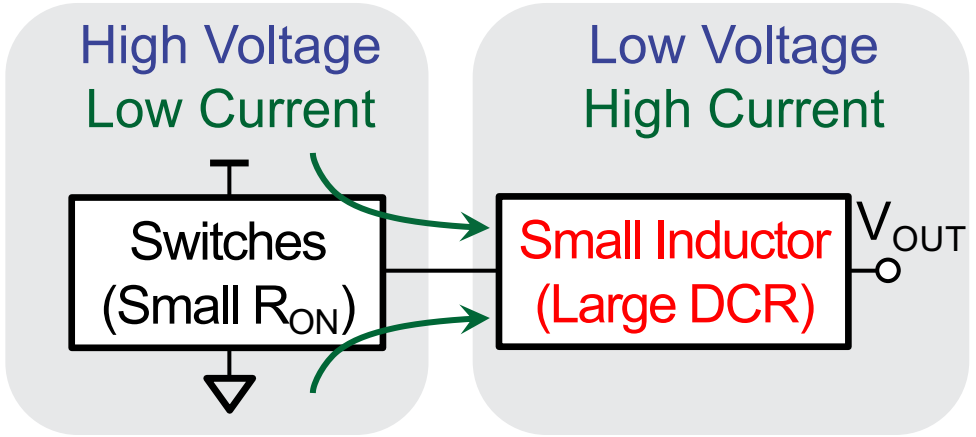
Total footprint (including inductor):
PD << 1W/mm²

Challenge:
Shrinking inductor increases losses

Building Up The PS3B Converter

- Starting from a conventional buck converter:





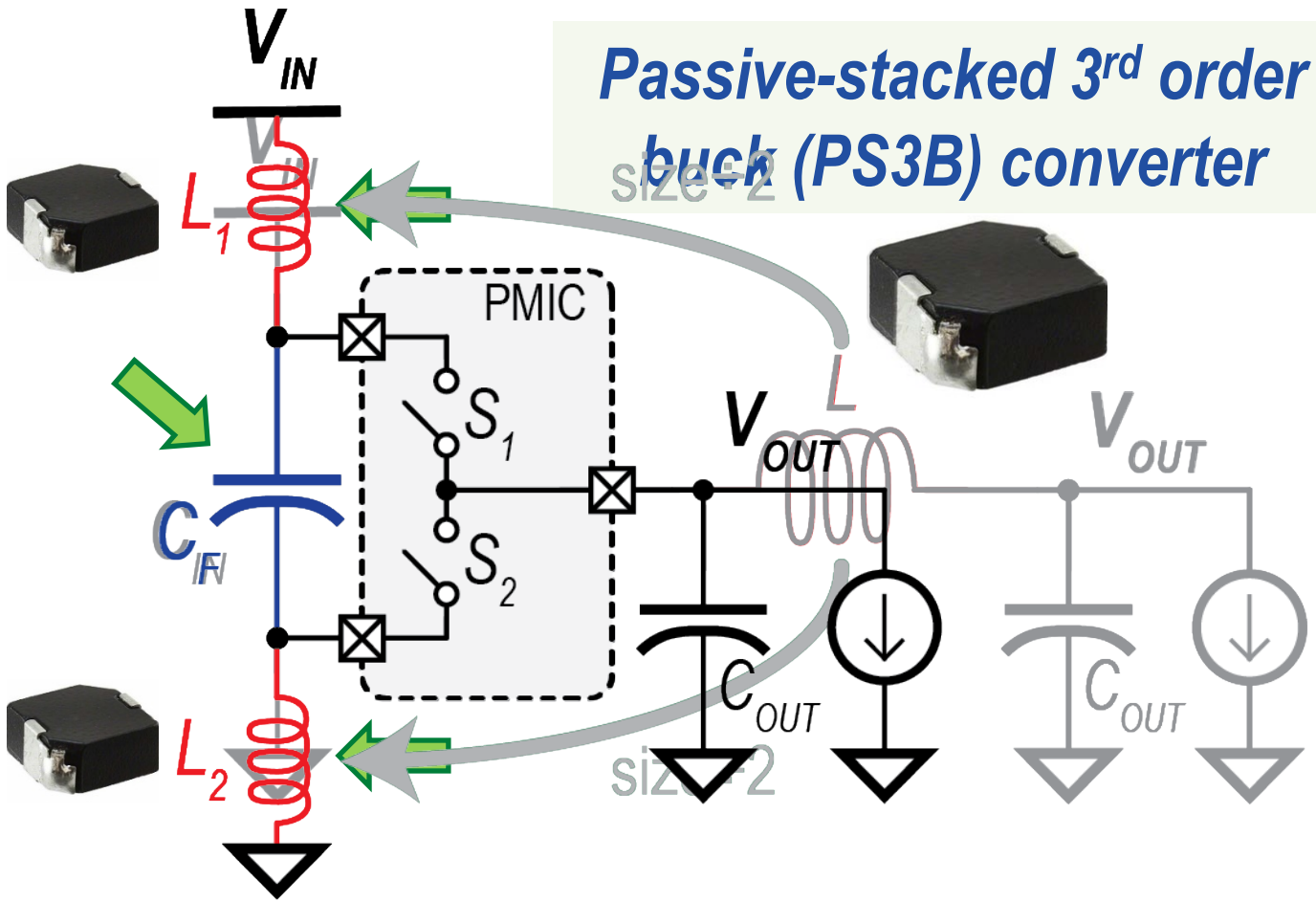
$$V_{IN}I_{IN} \approx V_{OUT}I_{OUT}$$

$$I_{OUT} > I_{IN}$$

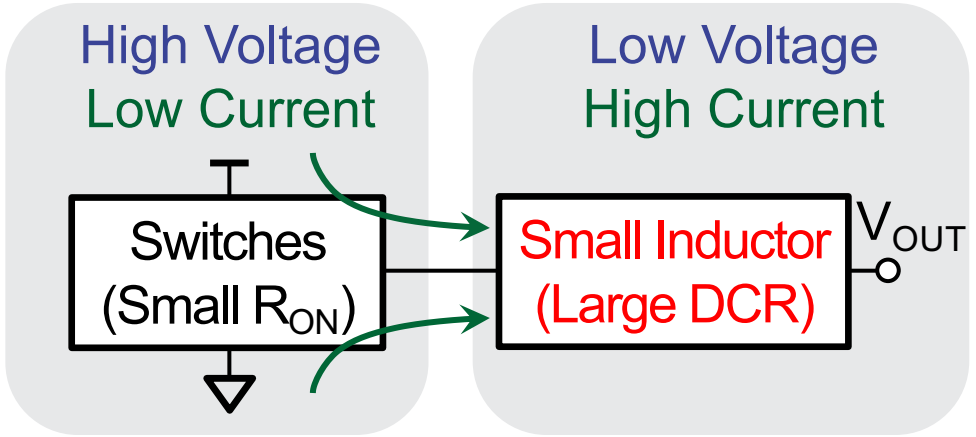
Inductors are placed at the high-current side of the converter

Building Up The PS3B Converter

- Moving the inductor to the input-side:



Passive-stacked 3rd order buck (PS3B) converter



Split into two half-sized inductors and stack at input

The input capacitor is now flying

All passives are stacked at input

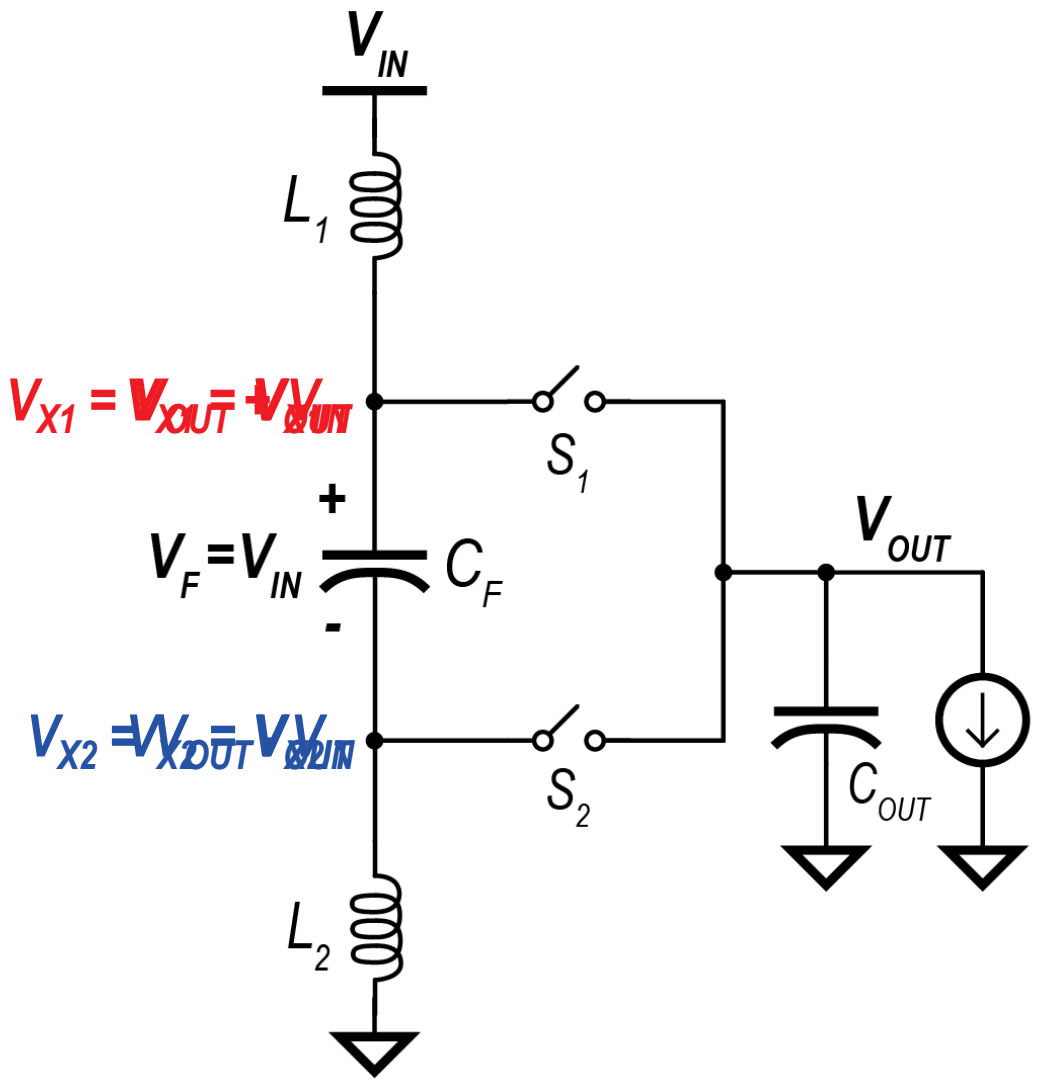
Inductors are placed at the low-current side of the converter

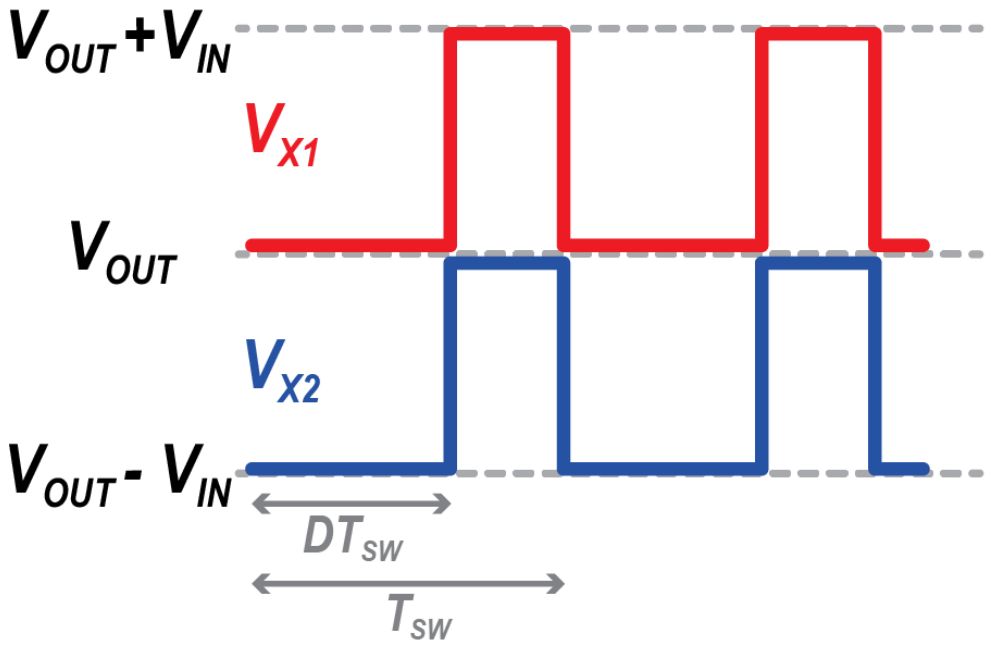
Outline

- Motivation
- PS3B Topology
  - Basic operation
  - Loss-related benefits
  - Noise-related benefits
  - Structure-related benefits
- Converter Implementation
- Measurement Results

Converter Basic Operation

- Voltage at switching nodes:

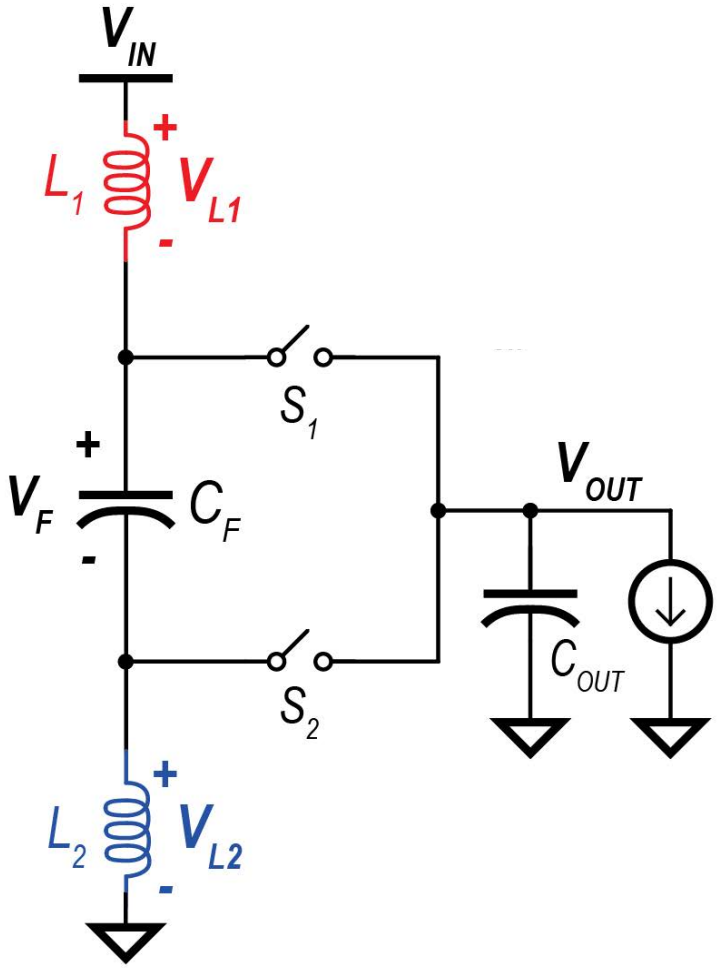




What is the relation between V_{IN} and V_{OUT} ?

Converter Basic Operation

- **Inductor volt-second relations:**



$$L_1: (V_{IN} - V_{OUT})D + (V_{IN} - V_F - V_{OUT})(1-D) = 0$$

$$L_2: (V_{OUT} - V_F)D + V_{OUT}(1-D) = 0$$

$V_F = V_{IN}$ $\quad$ $V_{OUT} = DV_{IN}$

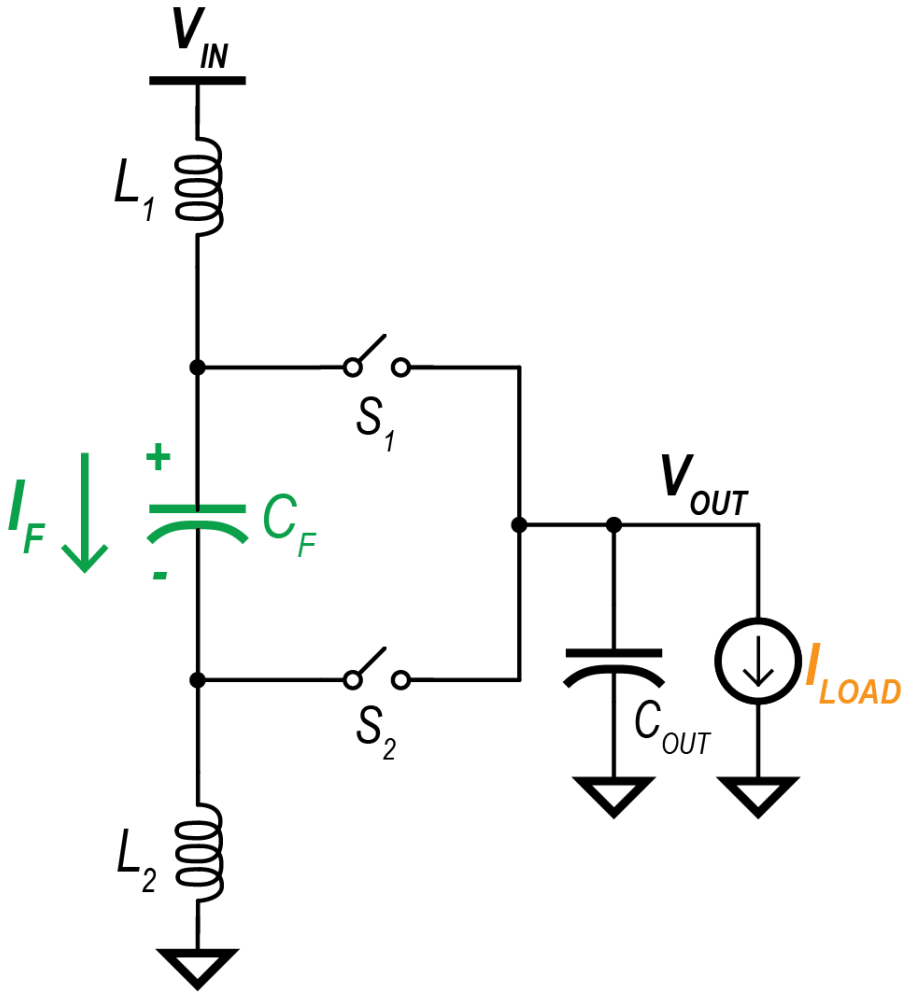
Relation between V_{IN} and V_{OUT} is the same as a buck converter

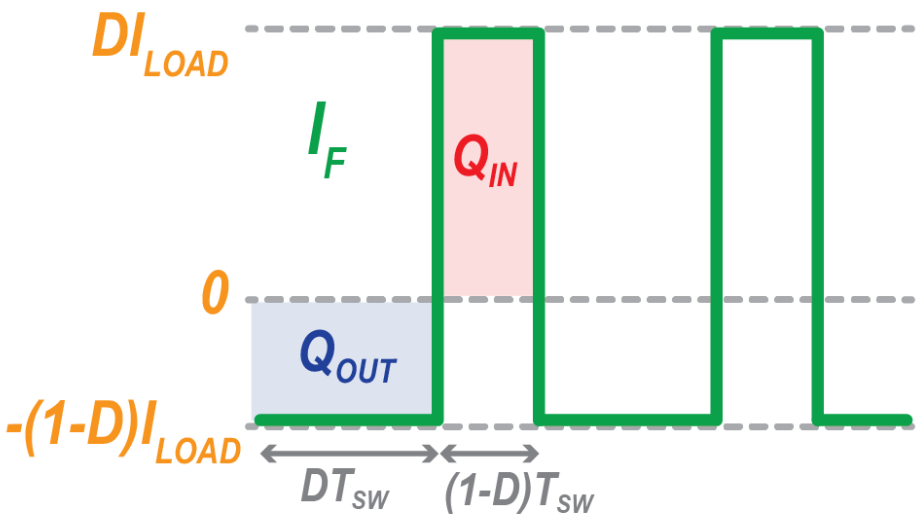
But achieved through 3 passive elements ⇨ ***Hence it is a 3rd order buck****

[*] R. Tymerski et al, *INTELEC*, 1986.

Converter Basic Operation

- **Flying capacitor stability:**





$$Q_{IN} = DI_{LOAD}\,(1-D)T_{SW}$$

$$Q_{OUT} = (1-D)I_{LOAD}\,DT_{SW}$$

$$Q_{IN} = Q_{OUT}$$

C_F is stable at V_{IN}

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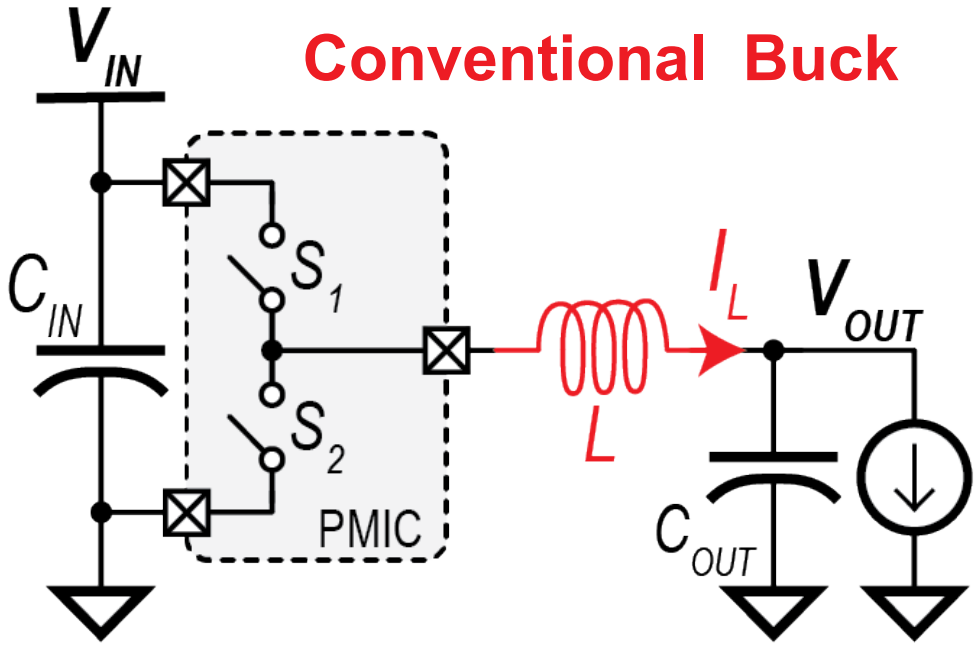
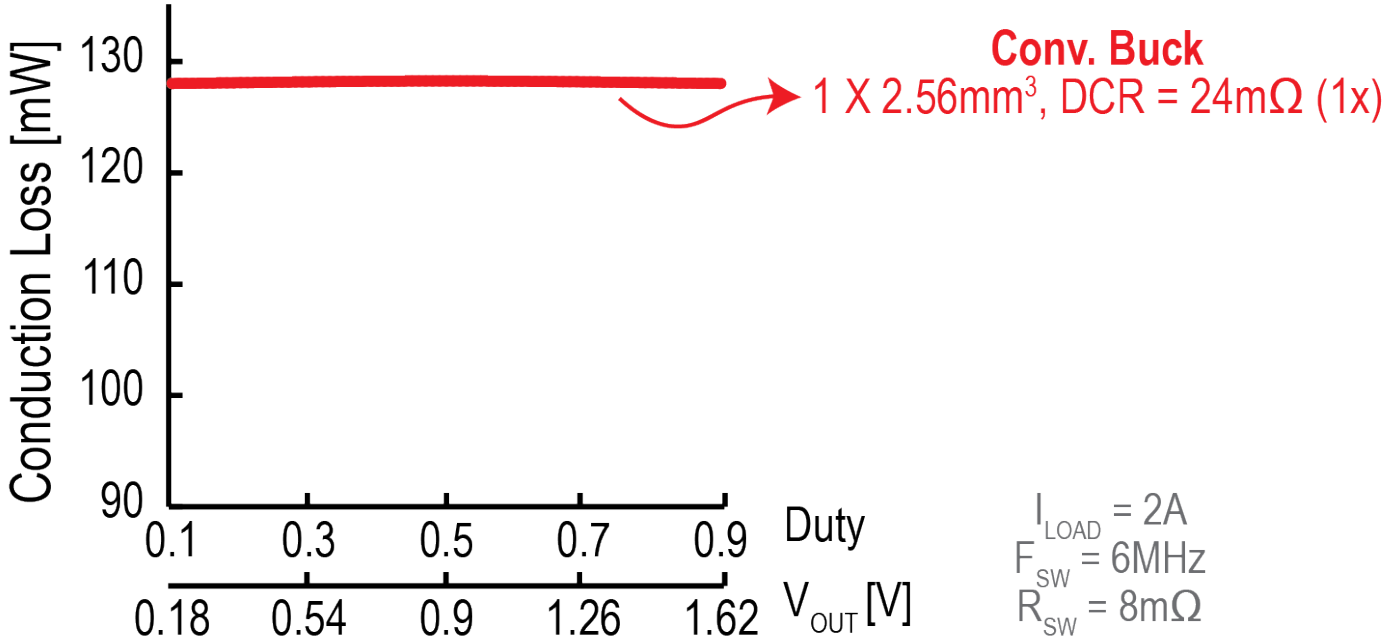
Loss-Related Benefits

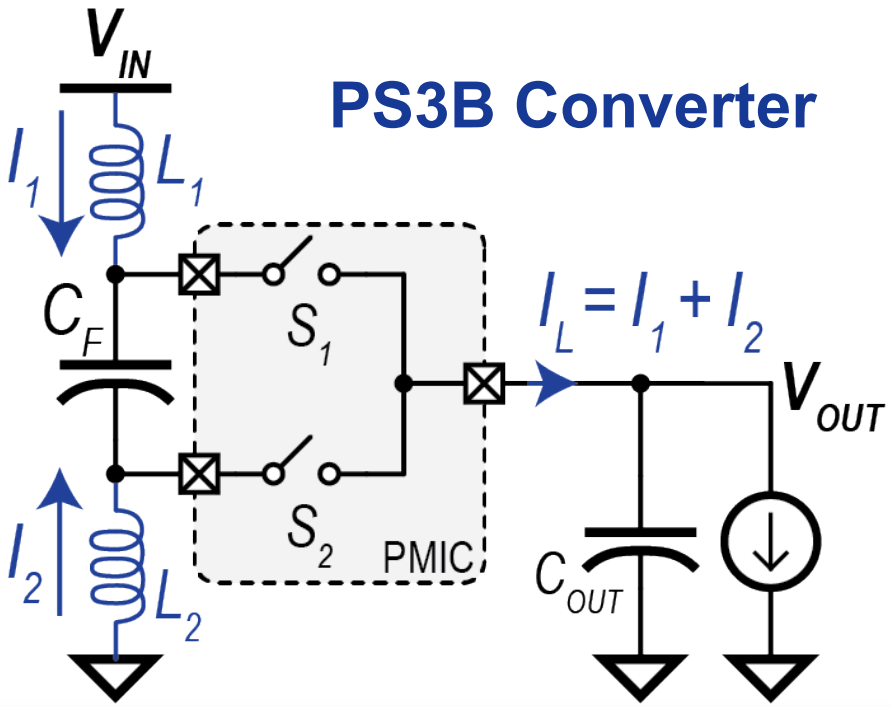
Conventional Buck



$$P_{LOSS,DCR,BUCK} = I_{RMS}^2 \times DCR \approx I_L^2 \times DCR$$



Loss-Related Benefits

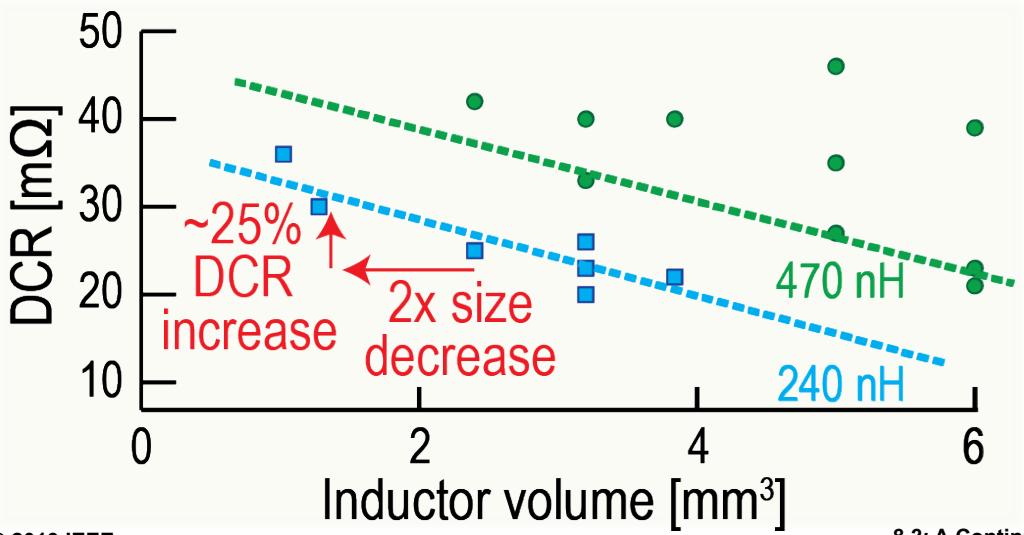


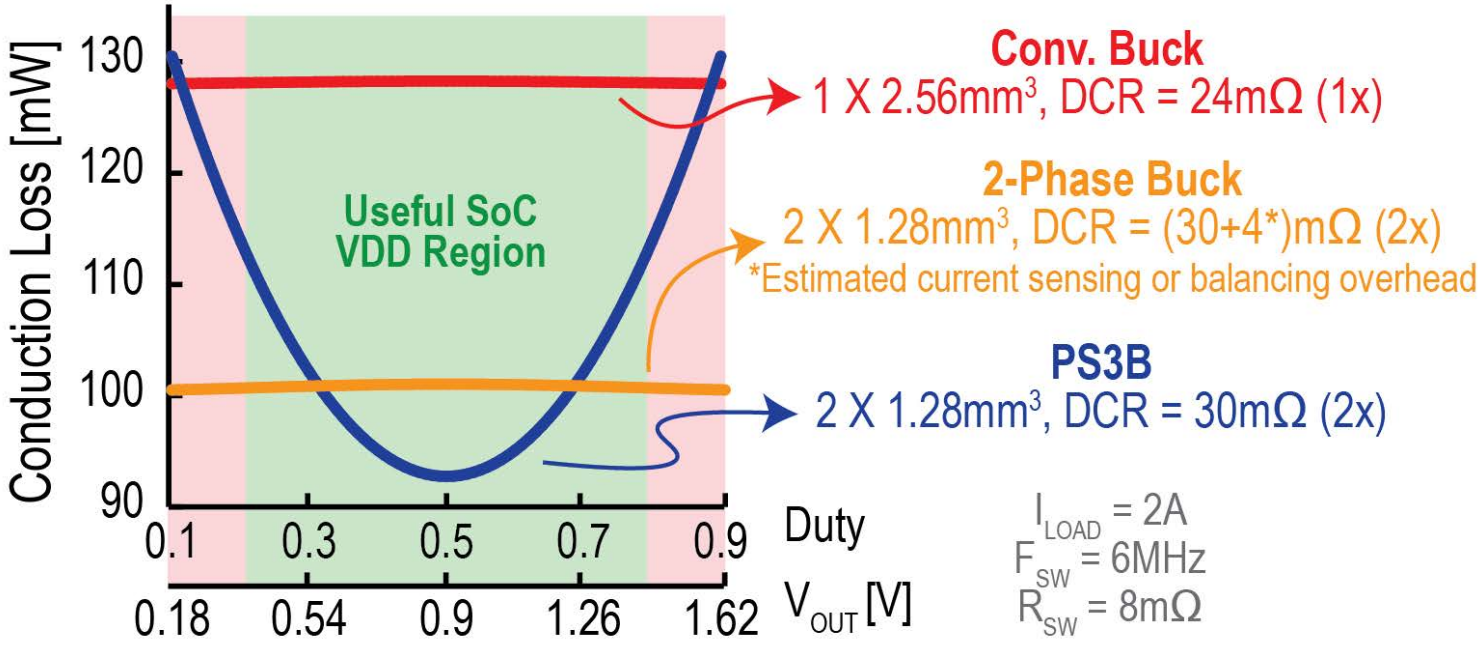
PS3B Converter

$$P_{LOSS,DCR,BUCK} = I_{RMS}^2 \times DCR \approx I_L^2 \times DCR$$

$$P_{LOSS,DCR,PS3B} = I_{RMS}^2 \times DCR \approx n \times I_L^2 \times DCR$$

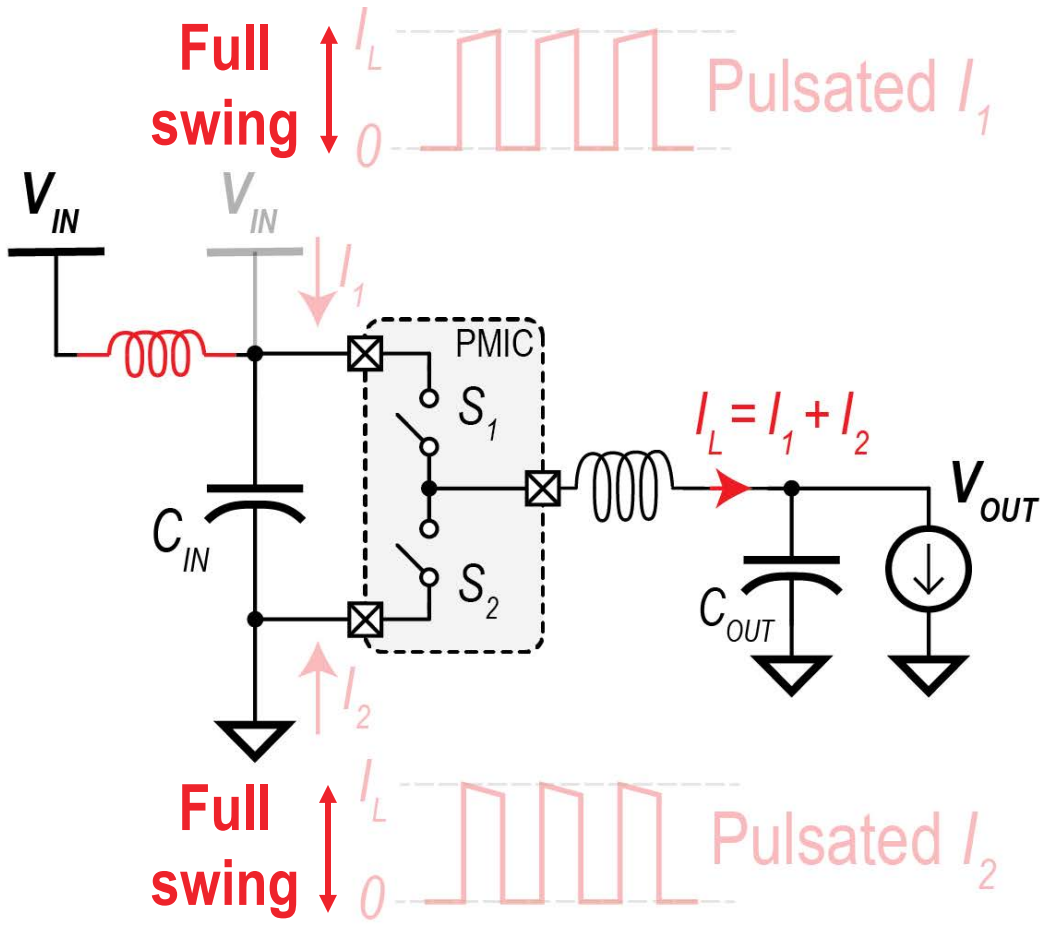
$$n = 1 - 2D + 2D^2 \rightarrow (0.5 < n < 1)$$





Noise-Related Benefits

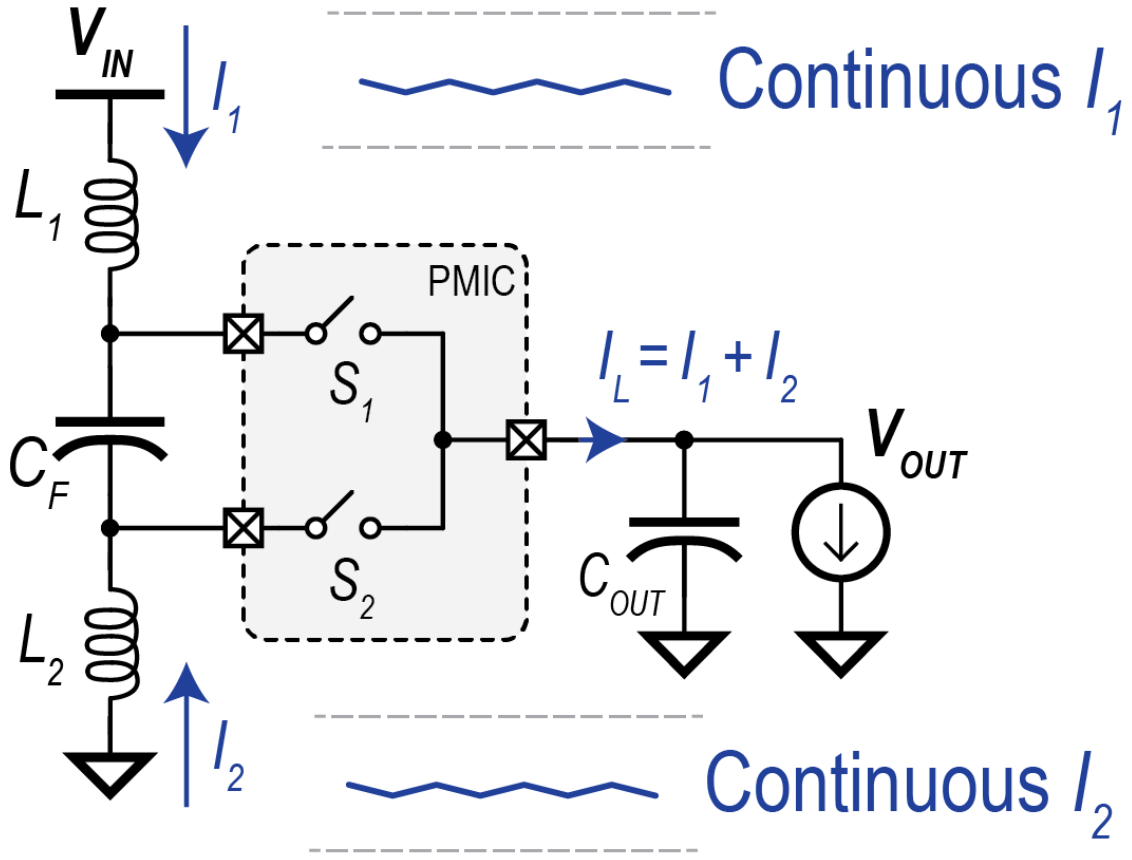
Conventional Buck



Noise and EMI at the input

Additional input filtering may be required

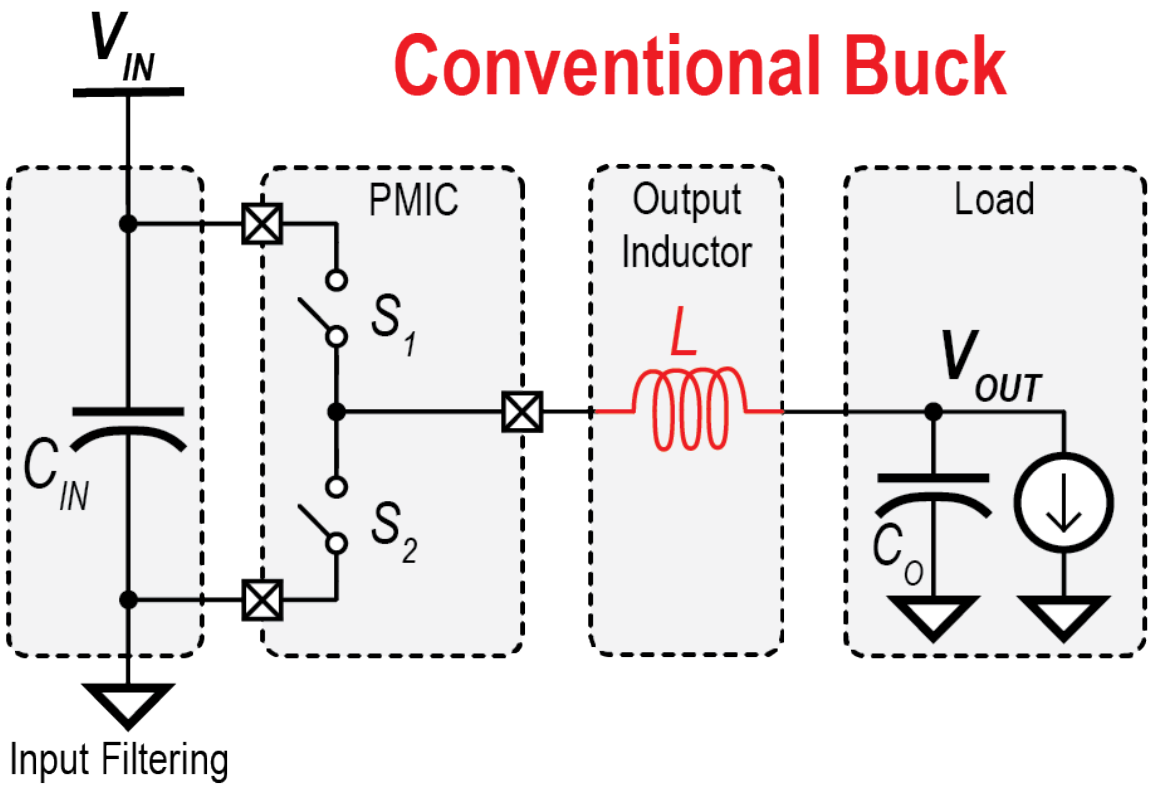
PS3B Converter

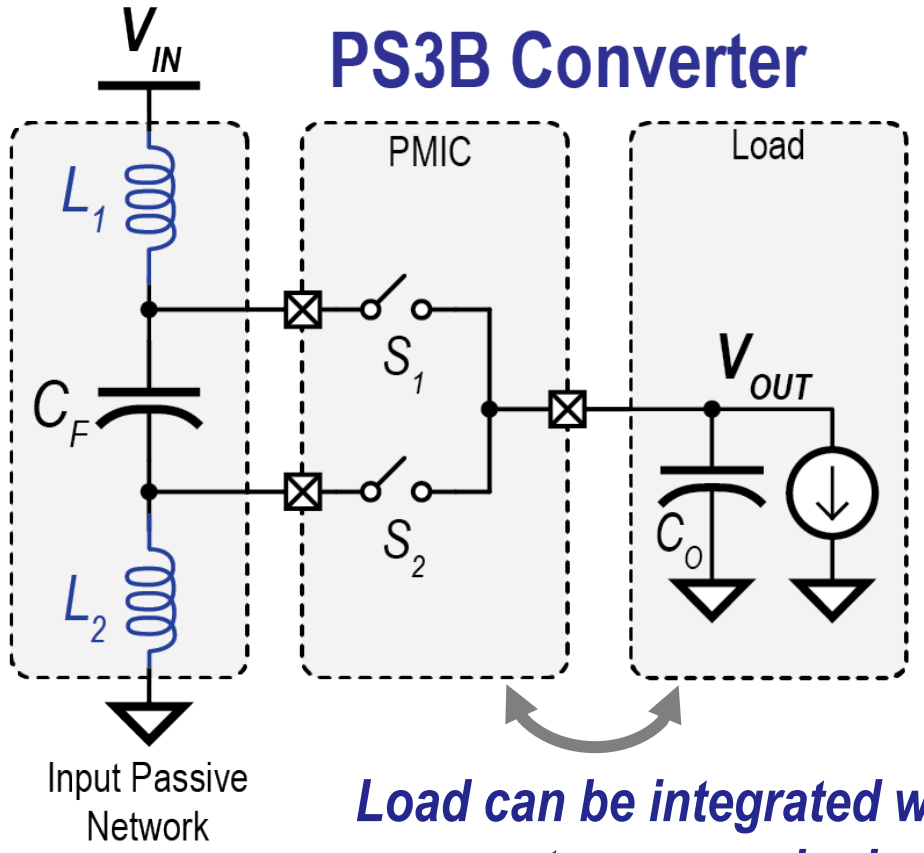


Substantially reduced noise and EMI at input

No need for input capacitor OR inductor

Structure-Related Benefits





Load can be integrated with power stage on a single die

The power stage and the load are separated by the output filter

Direct connection between the power stage and the load

Stacked passives minimize routing overhead

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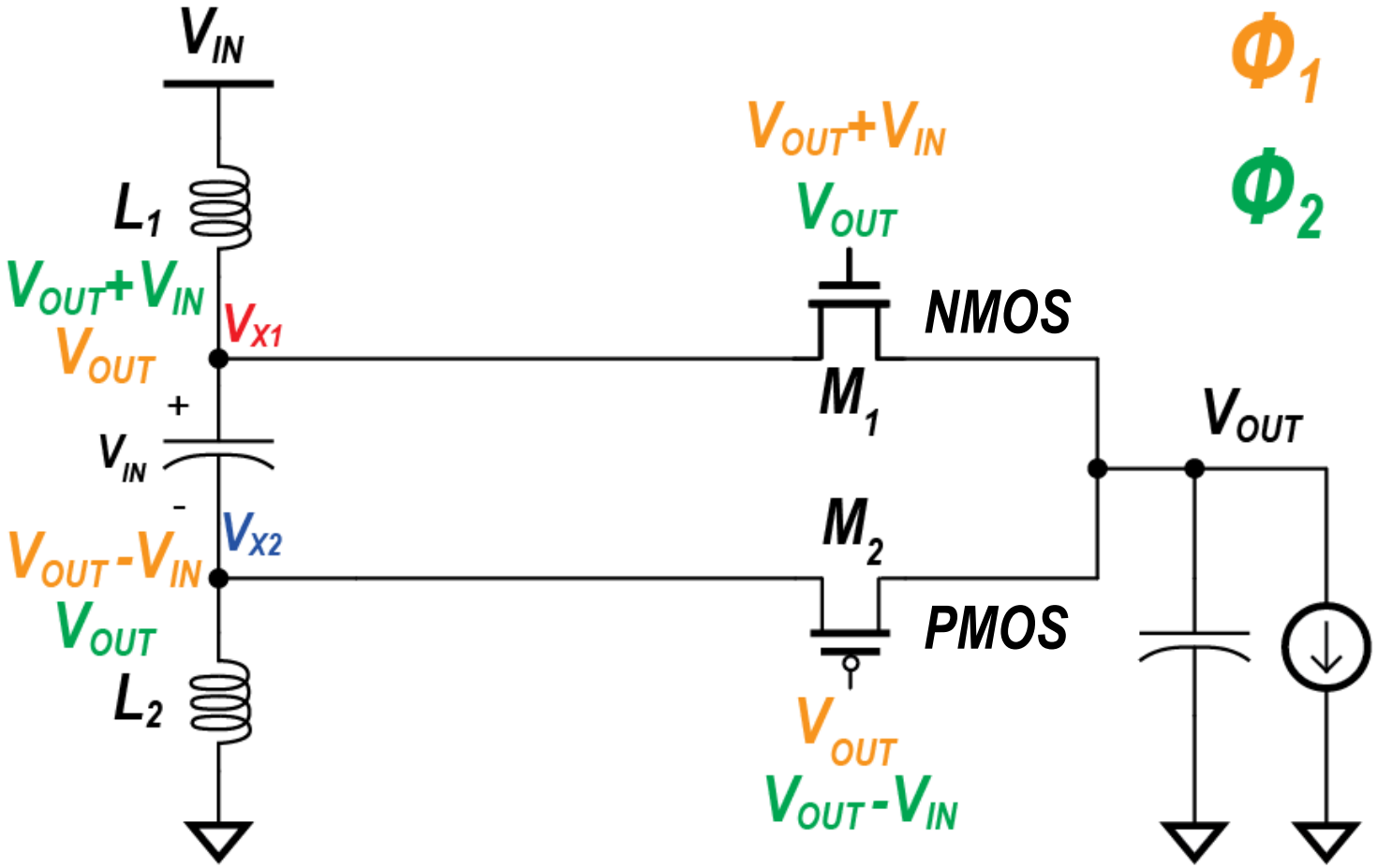
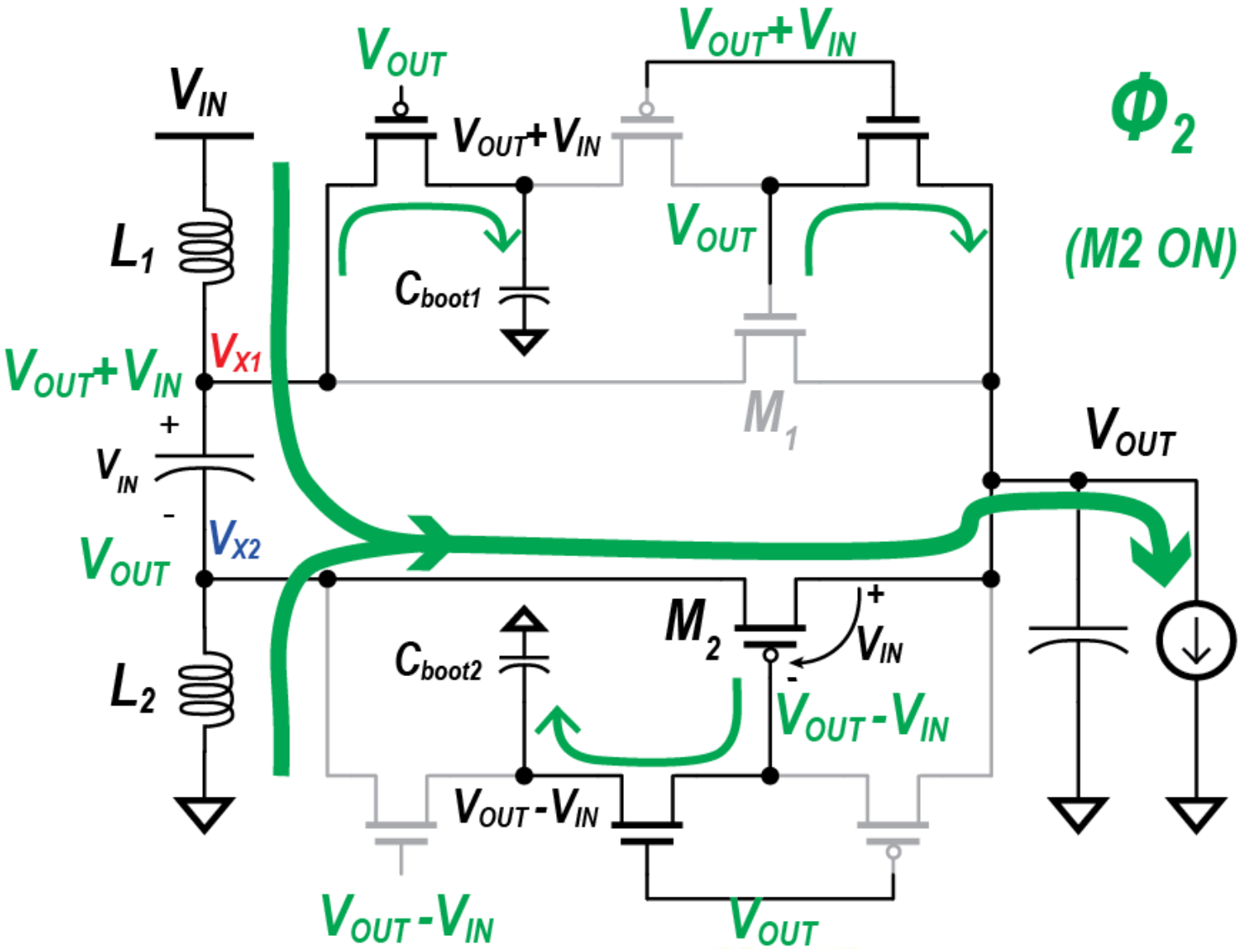
Implementing Power MOSFETs



Non-standard voltage levels are required to drive the power MOSFETs

These voltage levels are available at the two switching nodes V_{X1} and V_{X2}

MOSFET Drivers Using Bootstrapping Capacitors

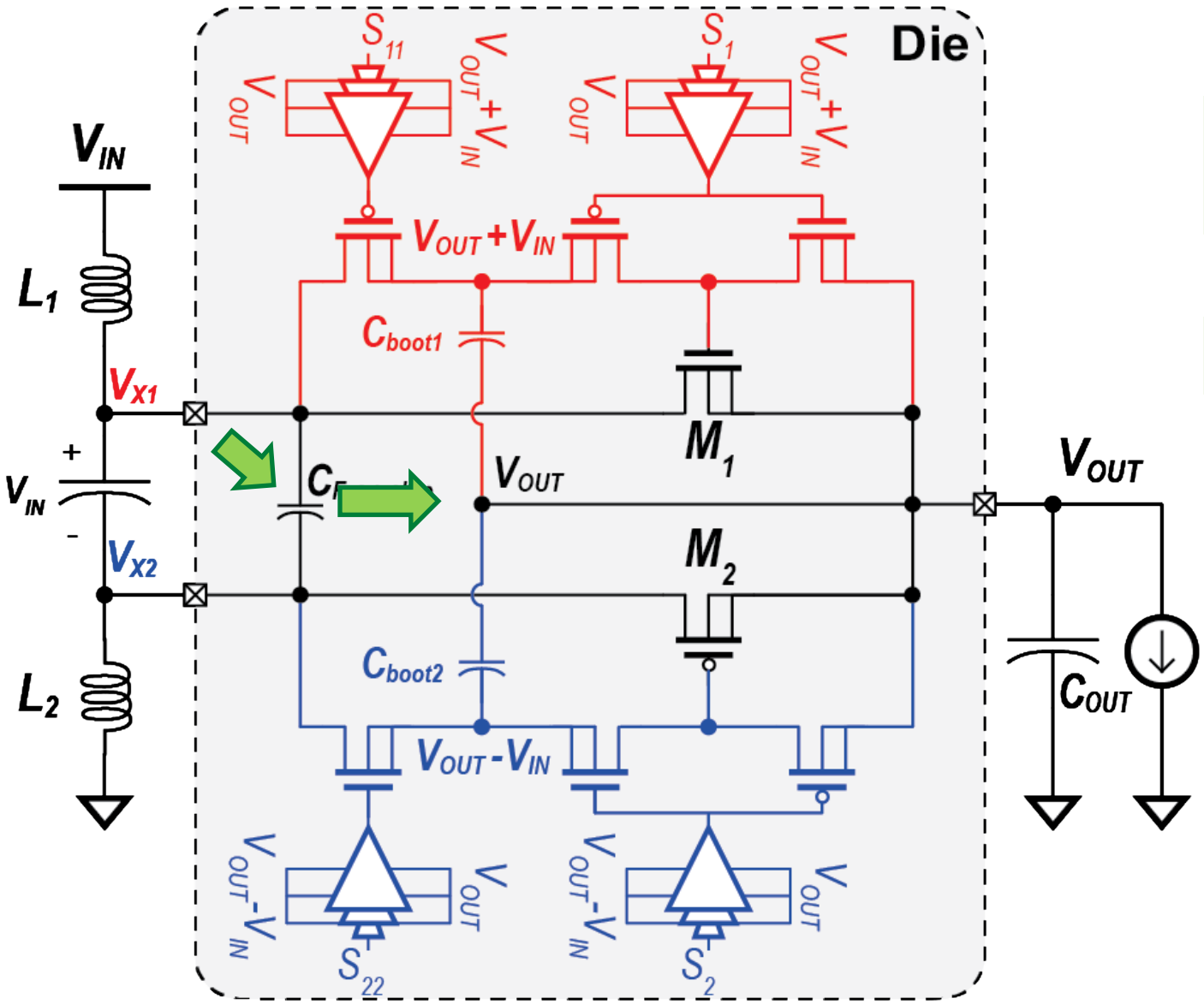


C_{boot1} stores the $(V_{OUT}+V_{IN})$ level and is used to drive M1

C_{boot2} stores the $(V_{OUT}-V_{IN})$ level and is used to drive M2

Power MOSFETs are driven from the internal nodes

Converter Full Schematic



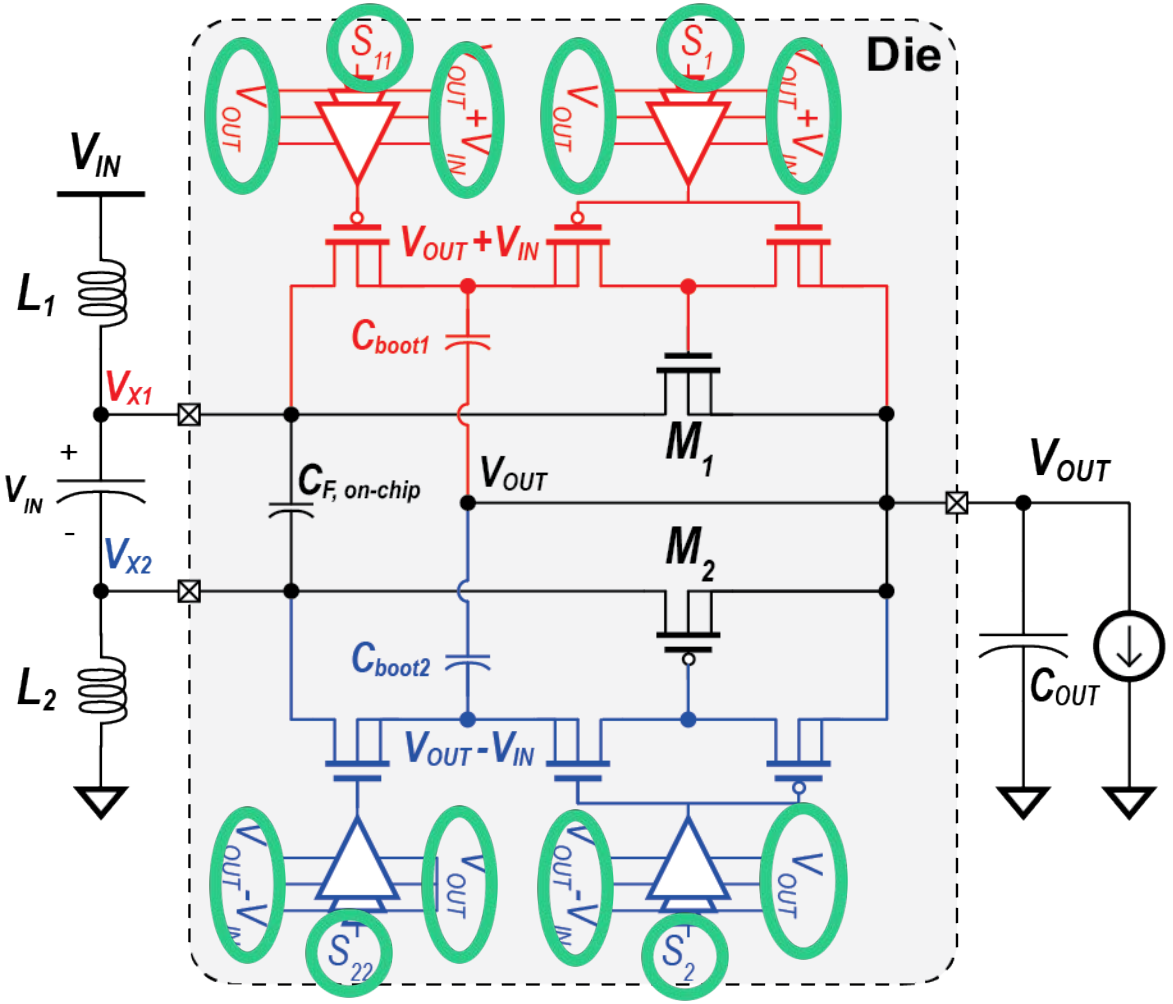
Bottom plate of C_{boot1} and top plate of C_{boot2} are connected to V_{OUT} instead of ground

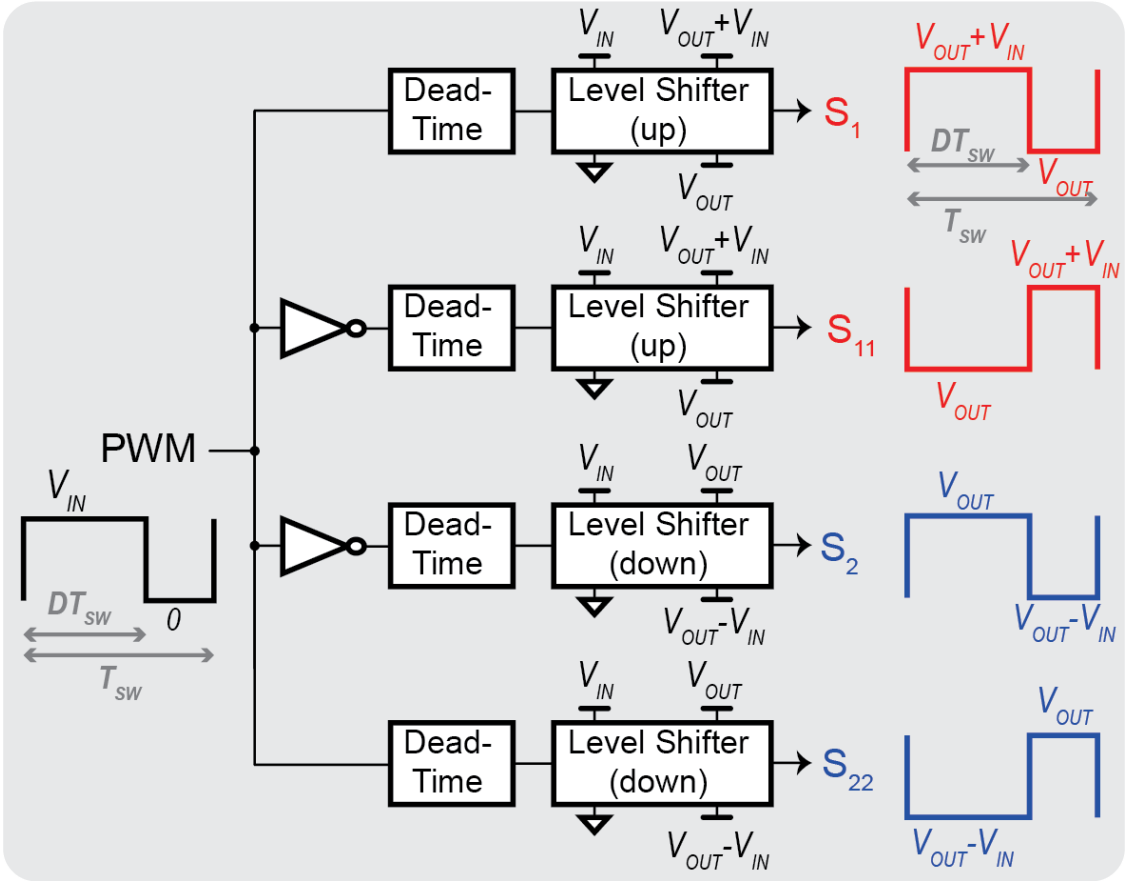
Both C_{boot1} and C_{boot2} block V_{IN} only

Up to 4x saving in capacitor implementation area

$C_{F,on\text{-}chip}$ is used to mitigate potential ringing on driver lines

Switch Drivers

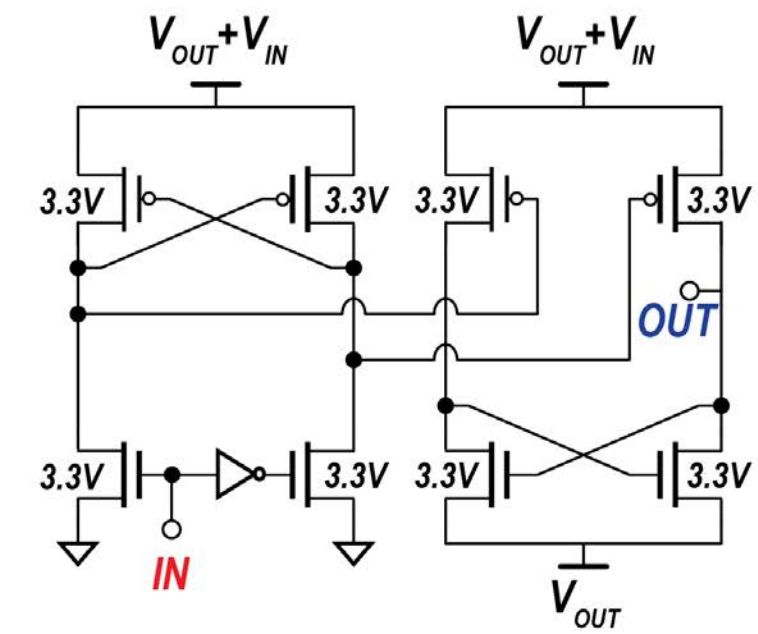


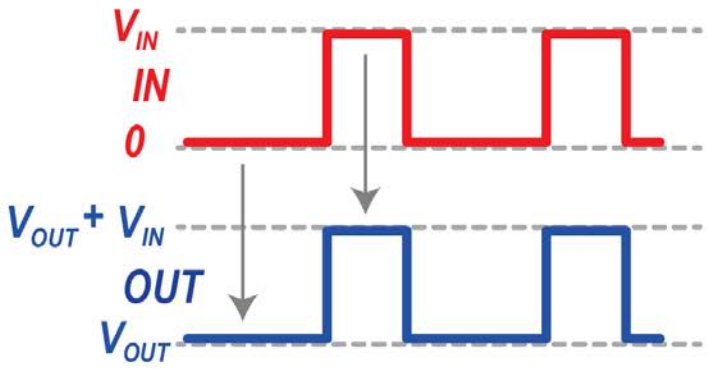


All the drivers are powered from the internal nodes of the converter

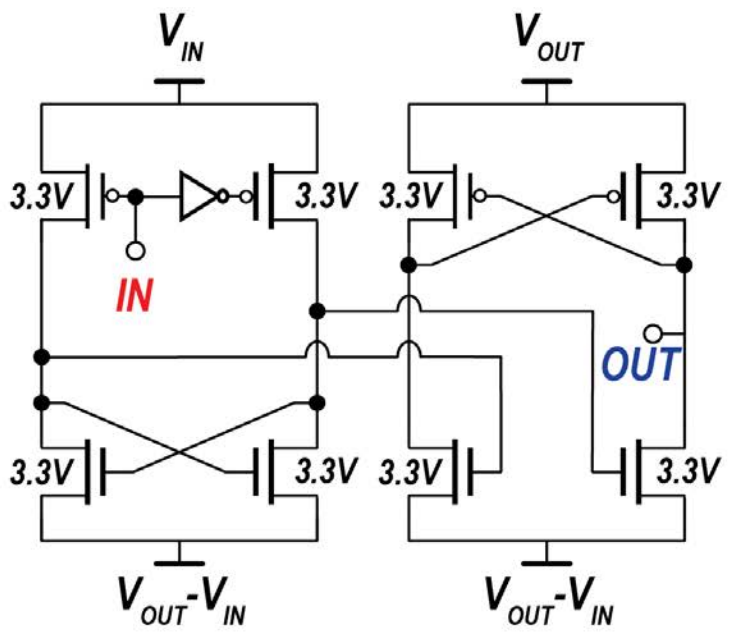
Four level-shifted control signals are generated from a single PWM signal

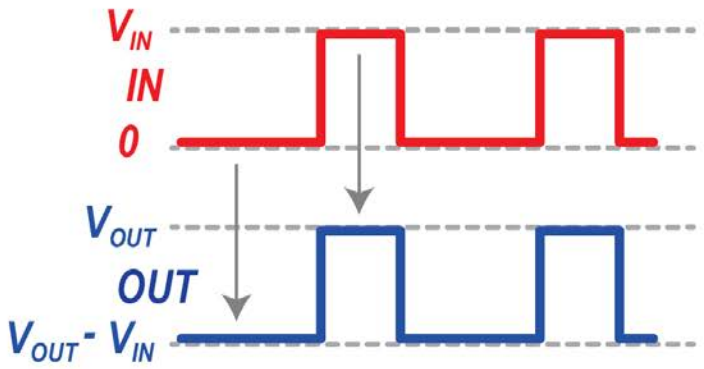
Level Shifters





Level Shifter (up)



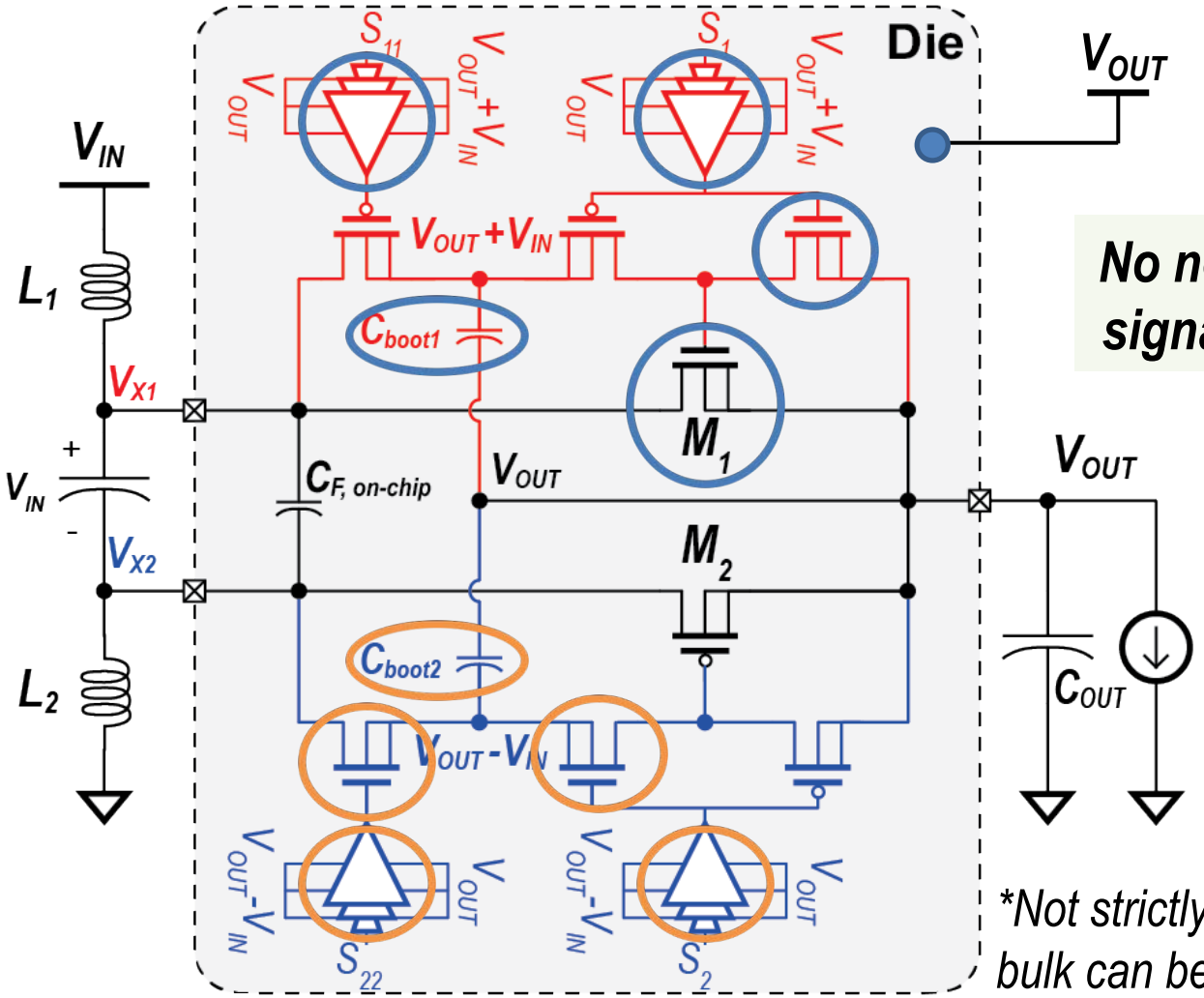


Level Shifter (down)

No need for external supplies for level shifters

PMIC Implementation

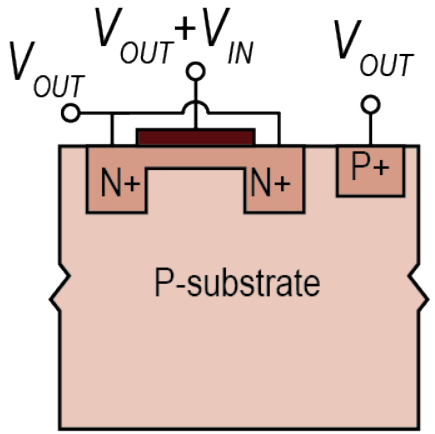
Standard devices



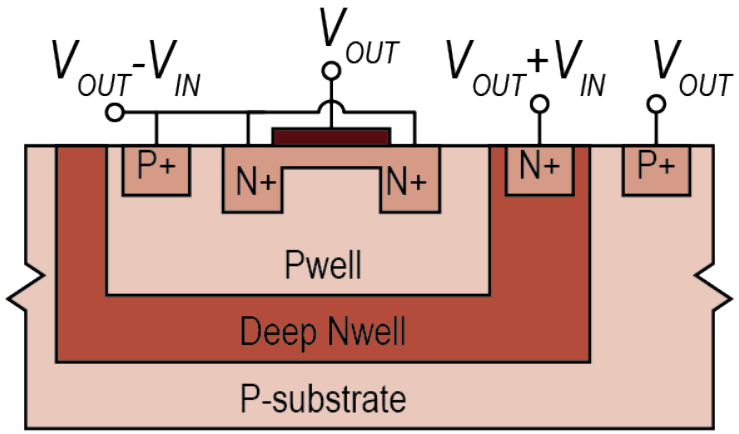
DNW devices

The chip bulk is biased to V_{OUT}*

No need for the ground signal inside the PMIC.



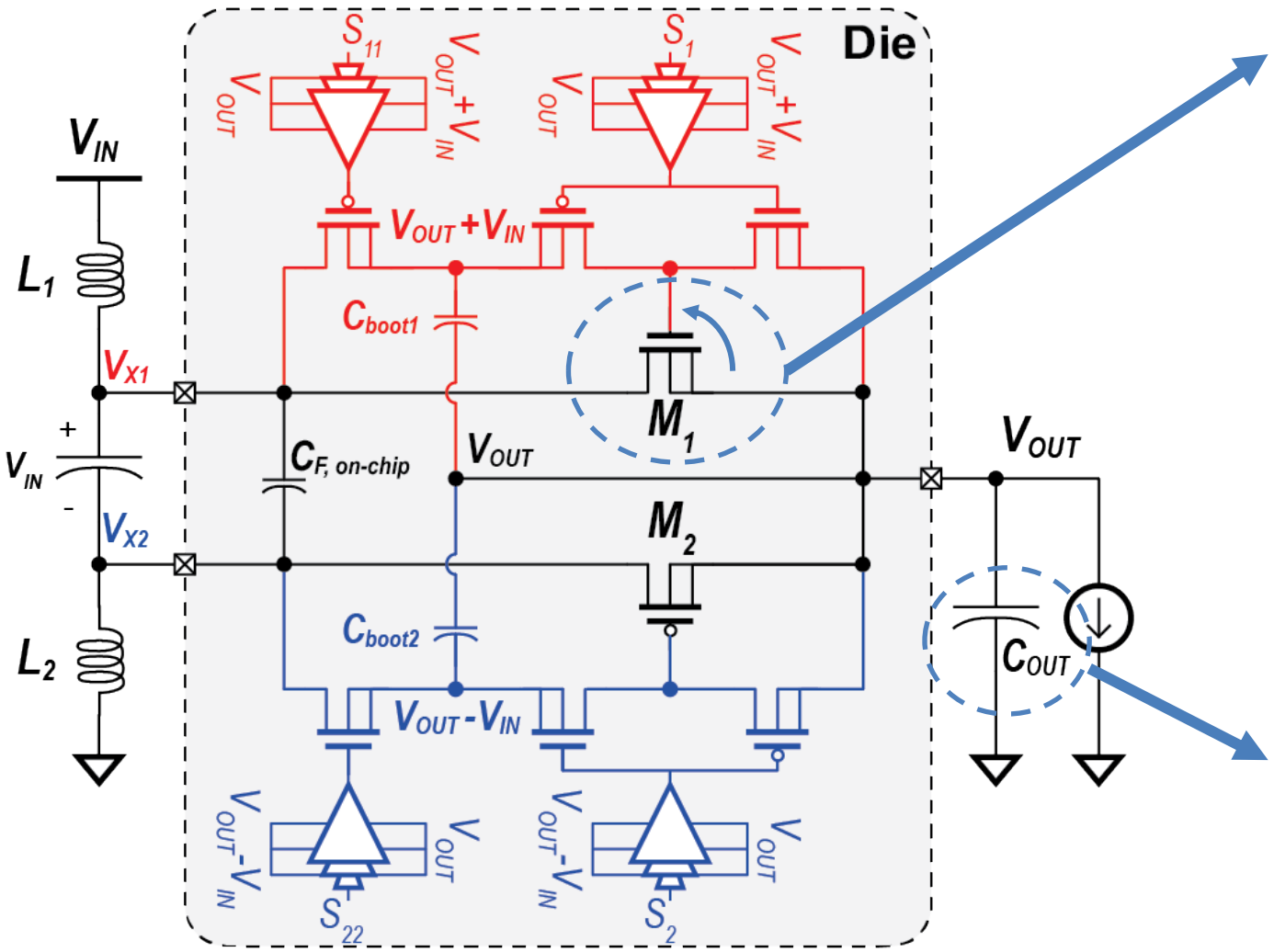
C_{boot1} Implementation



C_{boot2} Implementation

*Not strictly required, the chip bulk can be biased to ground but with more DNW devices.

PMIC Implementation

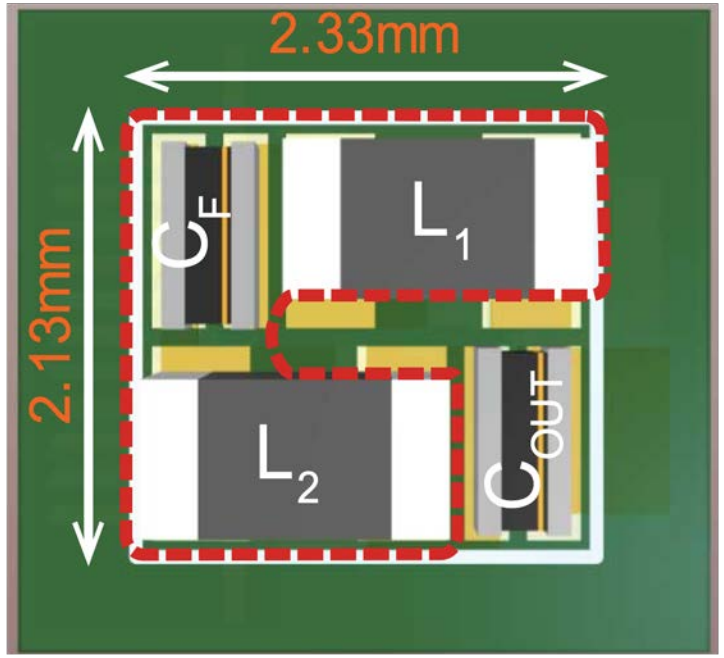


- Switching losses:
  - Parasitic capacitance of both power MOSFETs experience same ΔV as a buck converter.
  - PS3B and conventional buck converter have same switching losses.

- The current ripple at the output is doubled:
  - Need to use larger output capacitor.
  - In this design, 0.47µF was sufficient to get output ripples <30mV.

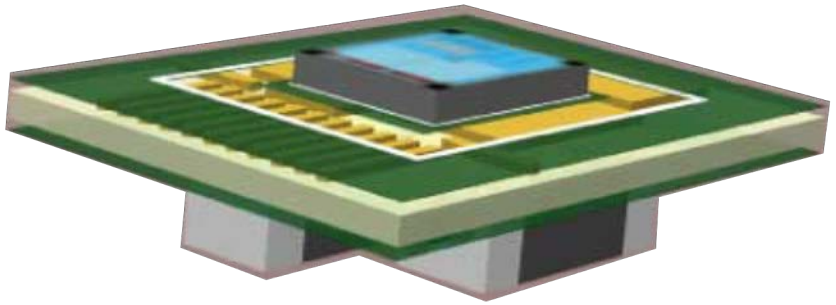
Converter Packaging

Total footprint: 5mm² including all the passives and the routing

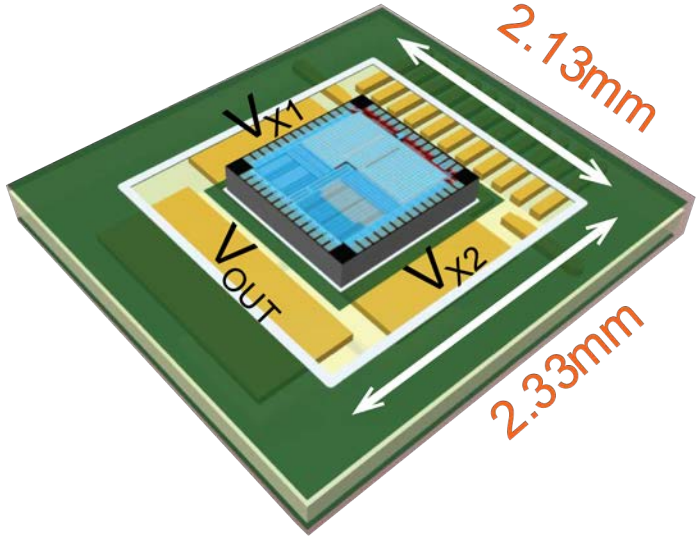


Passives stacked at the input allows for saving in the routing area

PMIC



Passives



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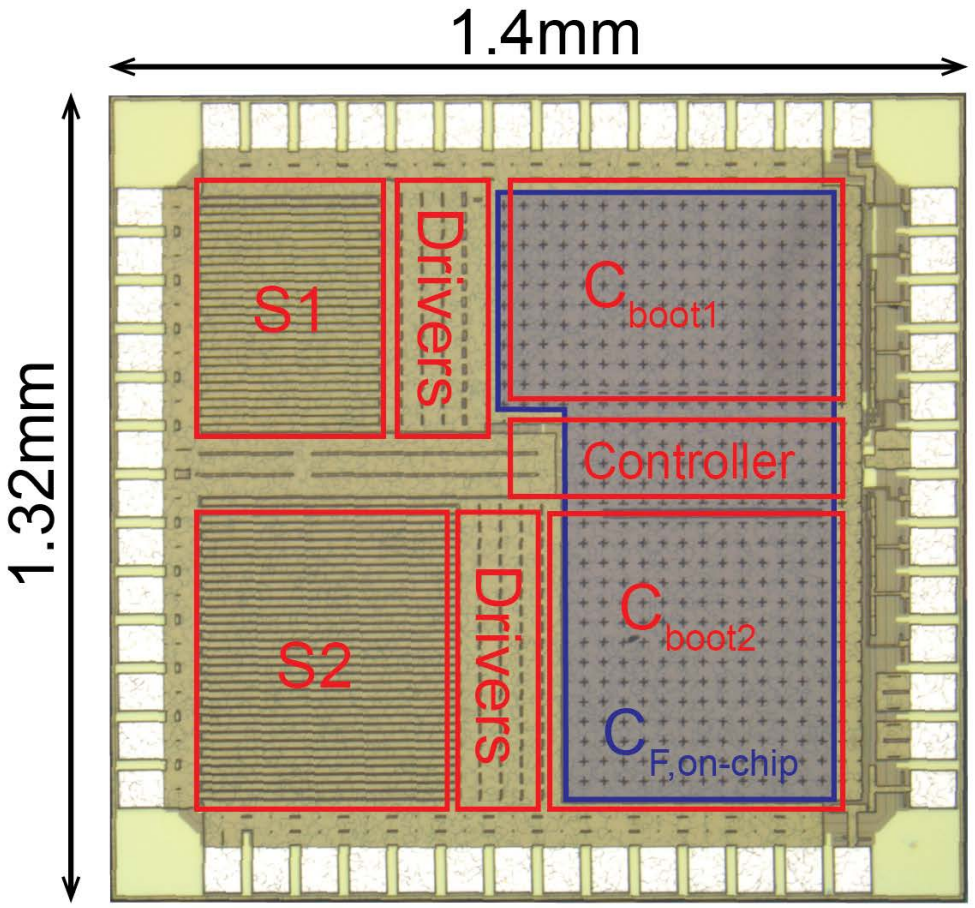
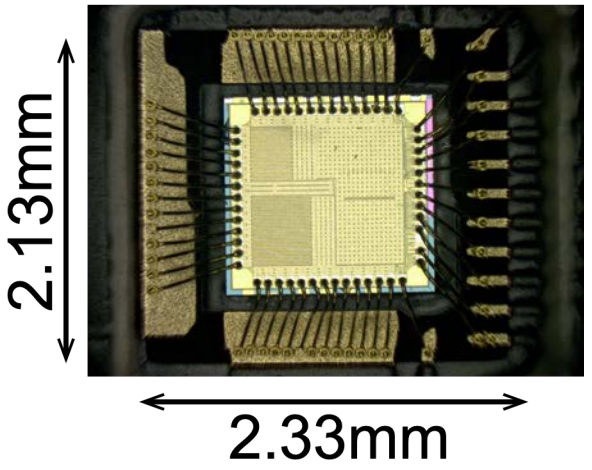
Die Photo and Converter Assembly

Chip Summary	
Process	0.18µm CMOS
PMIC Area	1.85mm²
VIN	1.8V
VOUT	0.5 – 1.5V
ILOAD	0.1 - 2.5A
FSW	6.5MHz

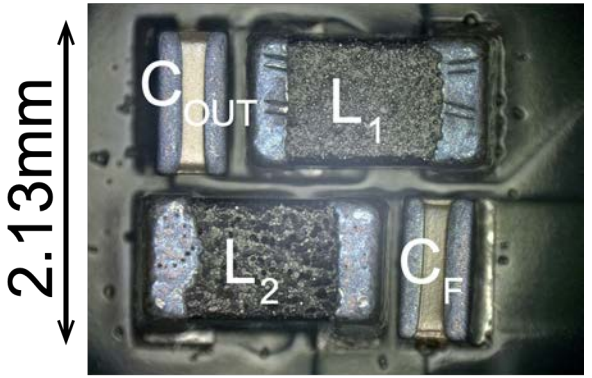


PMIC

Top-side

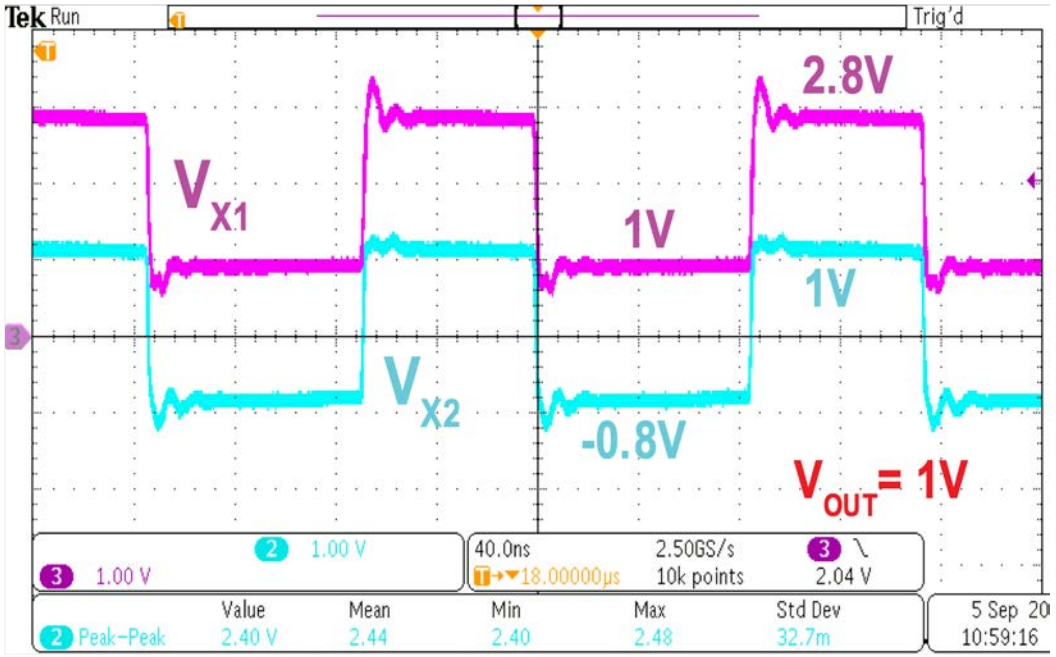


Bottom-side



Assembly

Measured Waveforms



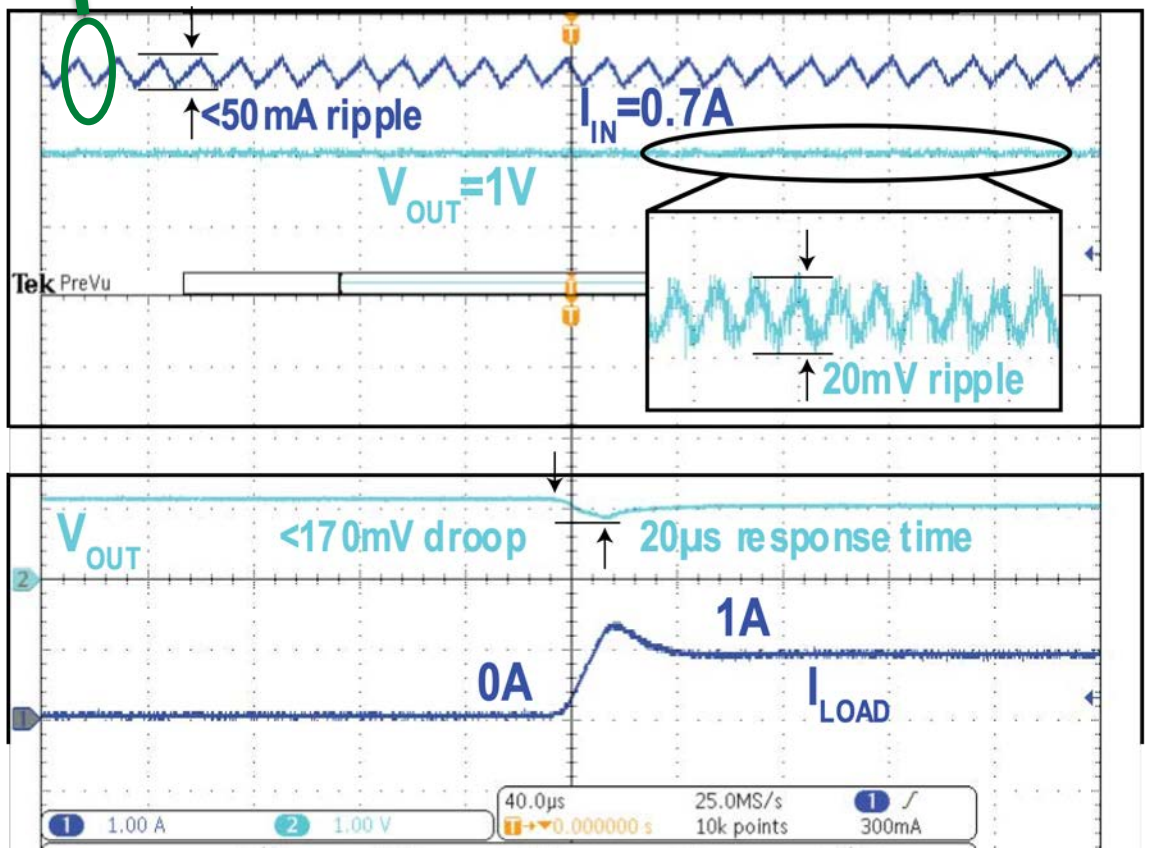
Switching nodes

V_{IN}=1.8V, V_{OUT}=1V
V_{X1}= 1V → 2.8V
V_{X2}= -0.8V → 1V

Correct levels for switching nodes

Continuous input current

Input current & output ripples

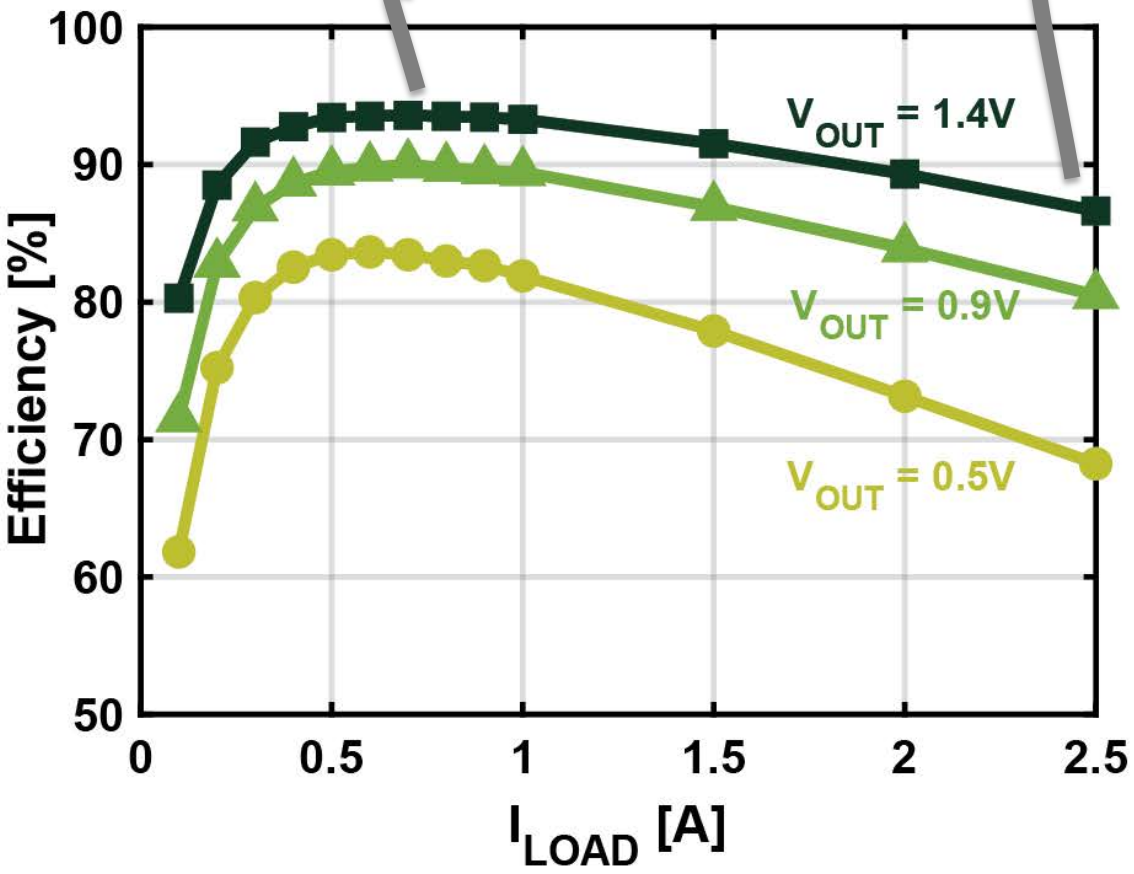


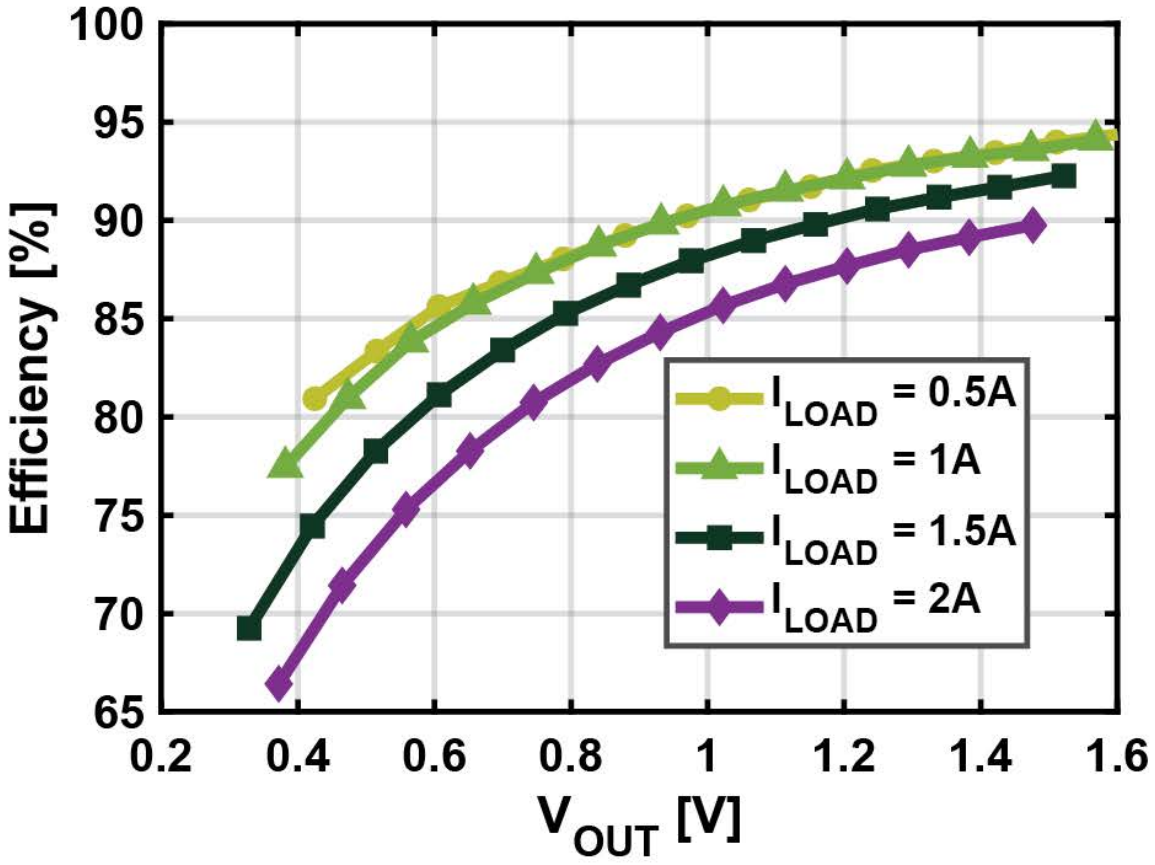
Transient response

Measured Efficiency

η_{peak}=94% @ PD of 0.18W/mm^2

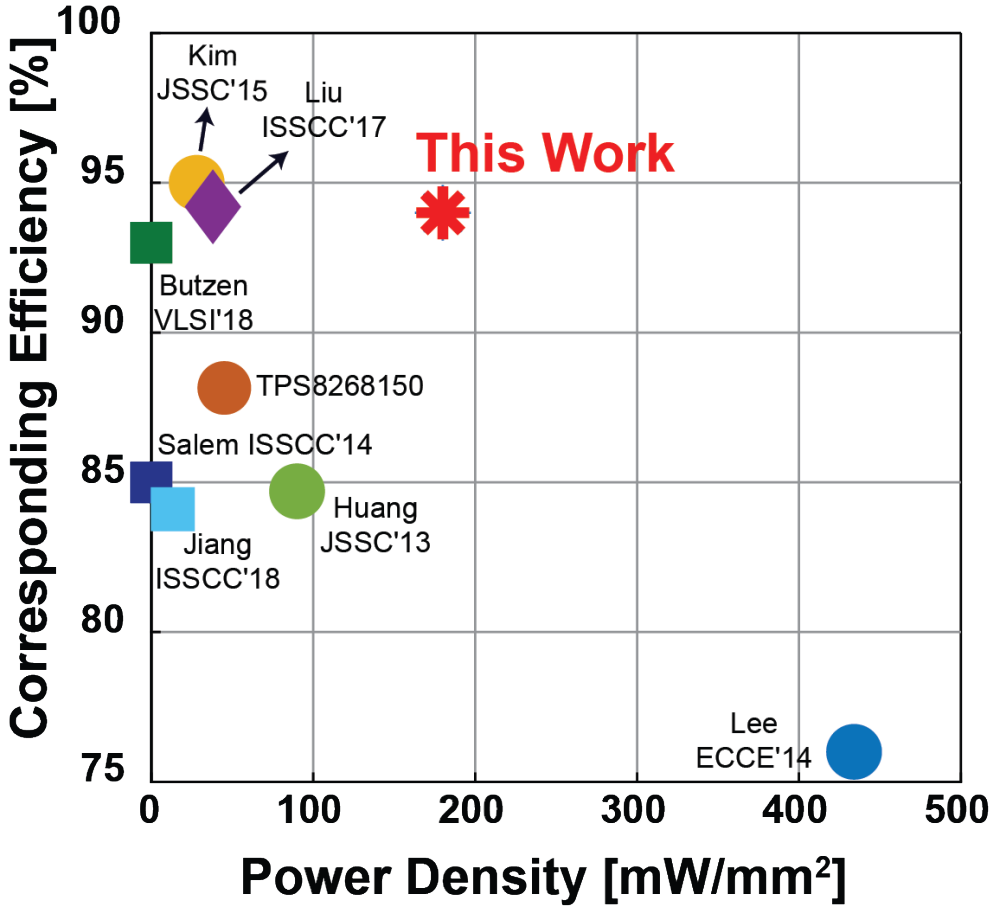
Max. PD of 0.7W/mm^2 @ 86.6%



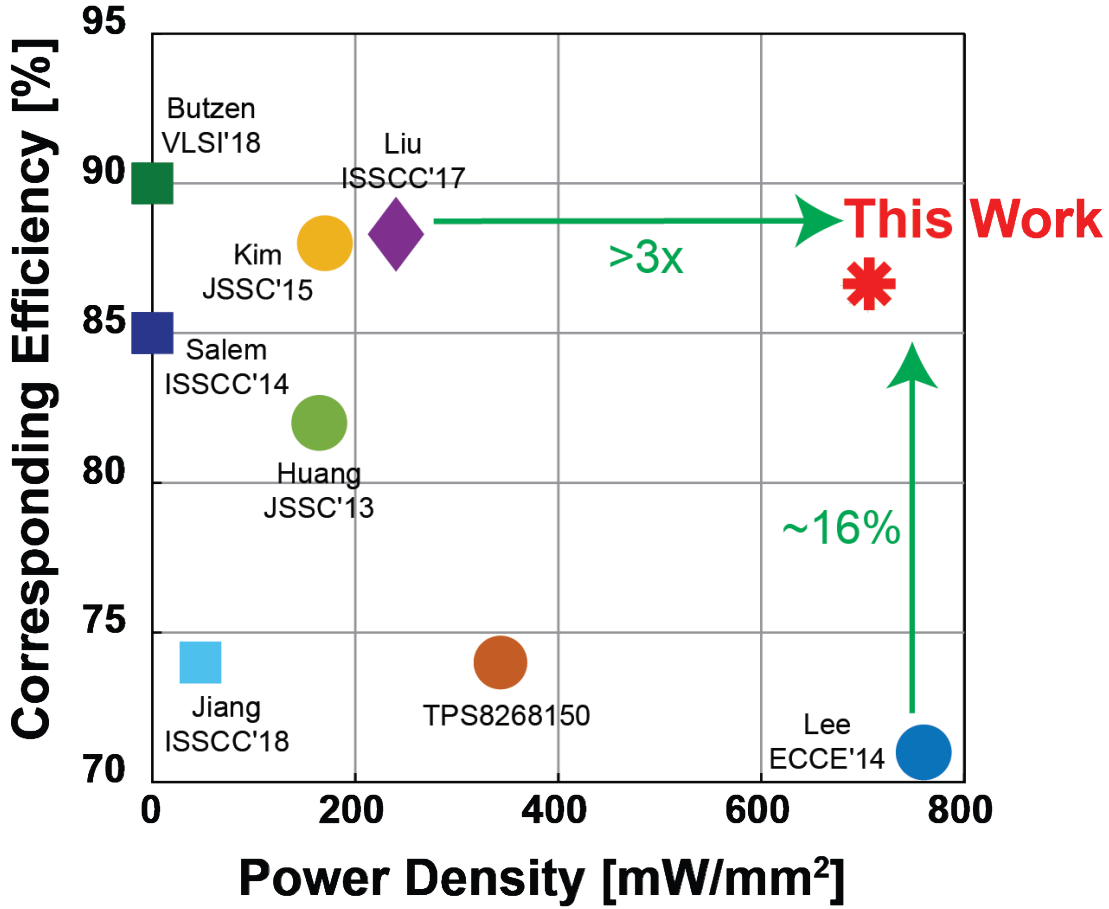


Power Density Comparison

Power Density @ Peak Efficiency (PE)



Efficiency @ Peak Power Density (PPD)



◆ Hybrid ■ SC* ● Conv. Buck

*Only switched-capacitor or resonant converters are shown with a high number of conversion ratios to mimic a continuous conversion ratio for DVFS-enabled voltage regulation.

Table of Comparisons

	Kim JSSC'15	Lee ISSCC'17	Liu ISSCC'17	Jia JSSC'18	Jiang ISSCC'18	TI TPS8268150	This Work
Topology	Buck	Buck (4-phase)	Hybrid (Multilevel)	Buck	SC (26 ratios)	Buck	**Hybrid (PS3B)**
Technology	65nm	350nm	65nm	65nm	65nm	NR	**180nm**
Input Voltage [V]	1.8	3.3	3.0 – 4.5	1.1	0.22 – 2.4	2.3 - 5.5	**1.8**
Output Voltage [V]	0.6 – 1.5	0.3 – 2.5	0.3 – 1.0	0.3 – 0.86	0.85 – 1.2	1.5	**0.5 – 1.5**
I_{LOAD} (MAX) [A]	0.6	6	1.53	0.04	0.08	1.6	**2.5**
Input Current	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	**Continuous**
PMIC Area [mm²]	5	1.88	4.05	0.13	2.42	6.67	**1.85**
Total Footprint [mm²]	5	NR	6**	0.13	2.42	6.67	**5**
Peak Efficiency (PE)	95.5%	88.1%	94.2%	73%	84.1%	88%***	**94%**
Power Density @ PE* [W/mm²]	0.03***	NR****	0.04**	NR	0.013	0.045***	**0.18 (0.25**)**
Peak Power Density (PPD)* [W/mm²]	0.17	NR****	0.24	0.27	0.034***	0.36***	**0.7 (1.0**)**
Efficiency @ PPD	88%	NR****	88.3%	NR	74%***	74%***	**86.6%**

* Unless otherwise specified, power densities are computed with respect to the total converter footprint including the passives and routing
** Computed by summing the area of the passive component footprints
*** Estimated from measurement results
**** The area of the passives are not reported

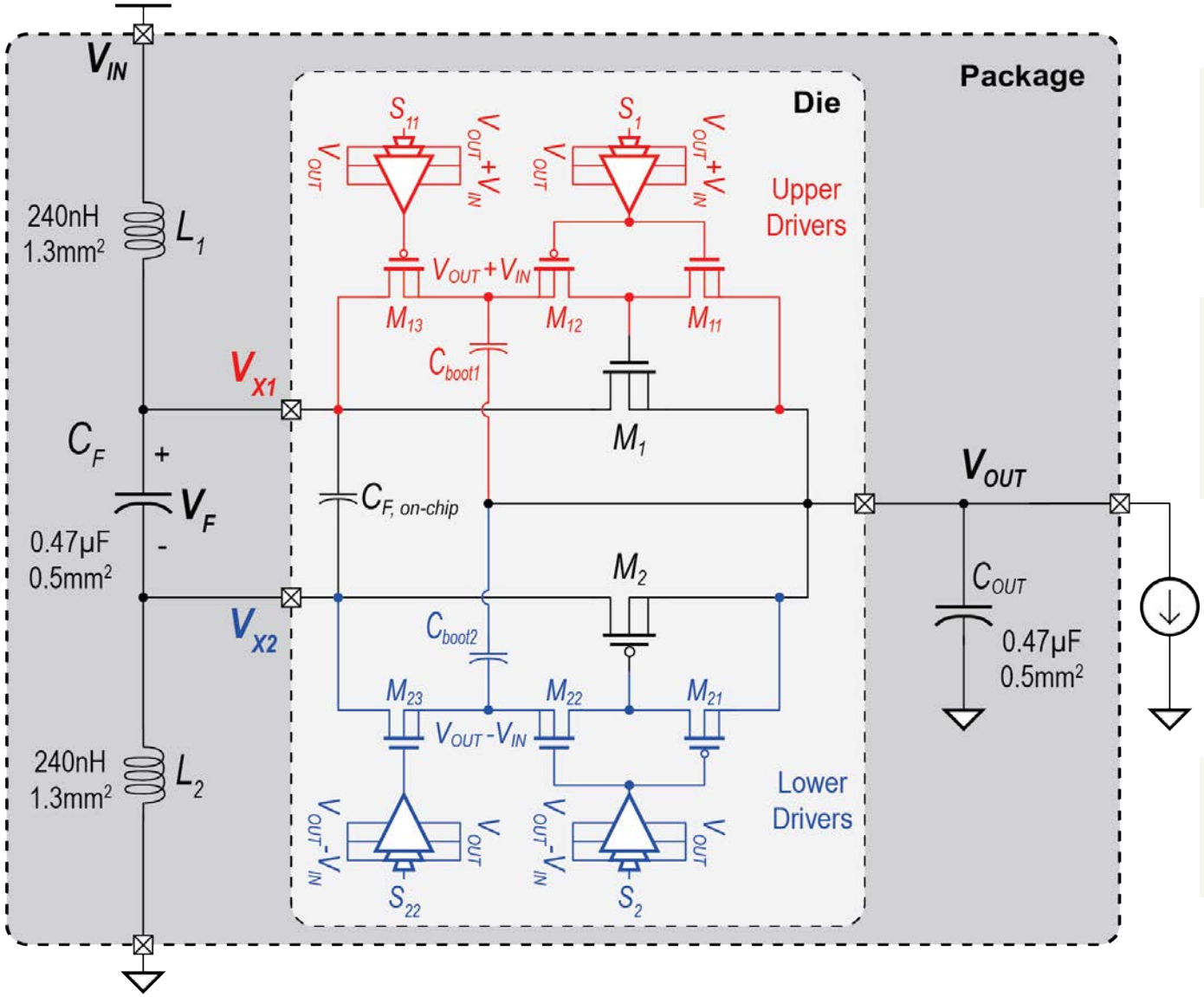
Summary

- ***A 3rd order buck is introduced:***
  - **Reduced conduction loss.**
  - **Continuous input current.**
  - **Small passives stacked at the input.**
- ***Achieves a high power density amongst prior-art converters that operate @ >85% efficiency with continuous conversion ratios across SoC-compatible voltage ranges.***
- **Achieves comparable peak efficiency (94%) @ >4x higher power density than prior-art.**
- **Has a unique feature of continuous input current, which would help minimize the area needed for on-board filtering.**

Acknowledgement: pSemi Corporation

Backup slides

Converter Full Schematic



Bottom plate of C_{boot1} and top plate of C_{boot2} are connected to V_{OUT} instead of ground

Both C_{boot1} and C_{boot2} block a V_{IN} only increasing their effective capacitance and reducing their required rating

Saving in capacitor implementation area of up to 4x

$C_{F,on\text{-}chip}$ is used to mitigate potential ringing on driver lines