A 51pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8Hz

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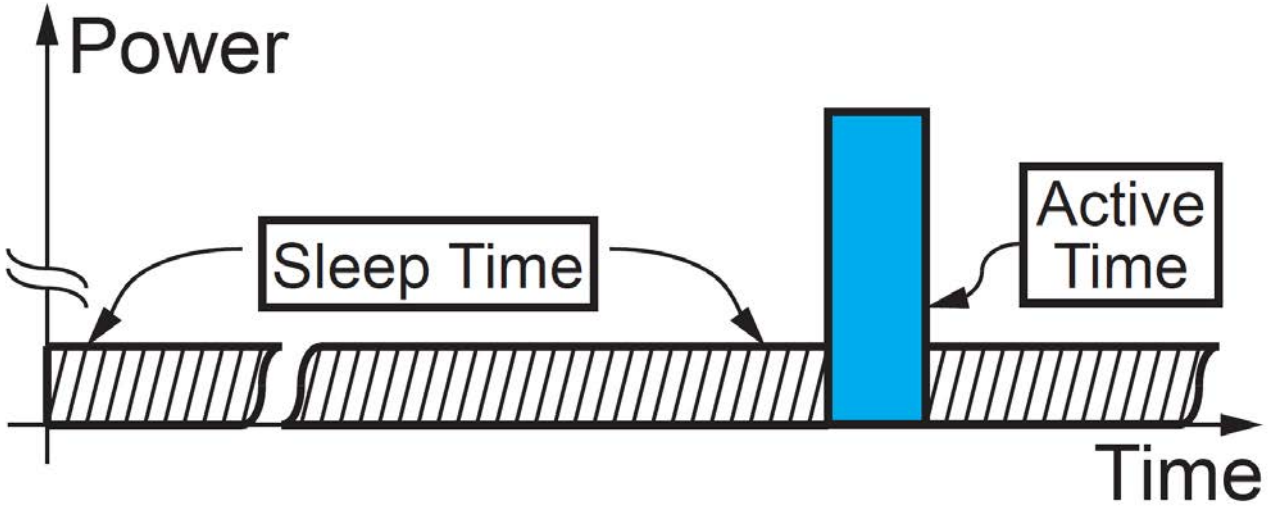
UCSD

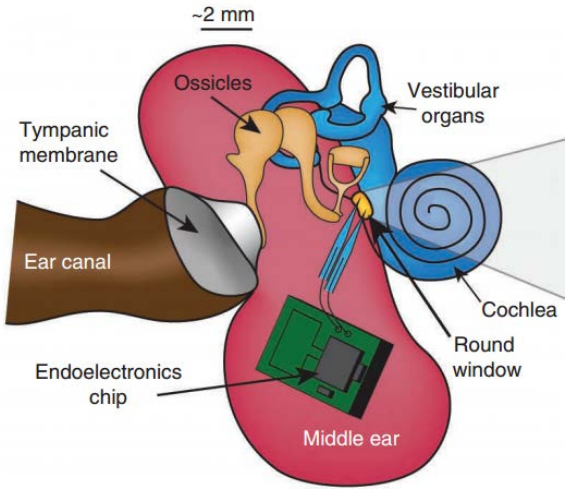
Wireless Sensing Platform

Long-Term Health Monitoring
- Blood glucose
- Gastric PH

Environmental Monitoring
- Temperature
- Water quality

Energy Harvesting
- Power extracted from the inner ear





Nature Biotechnology 2012
Courtesy of Prof. Patrick Mercier

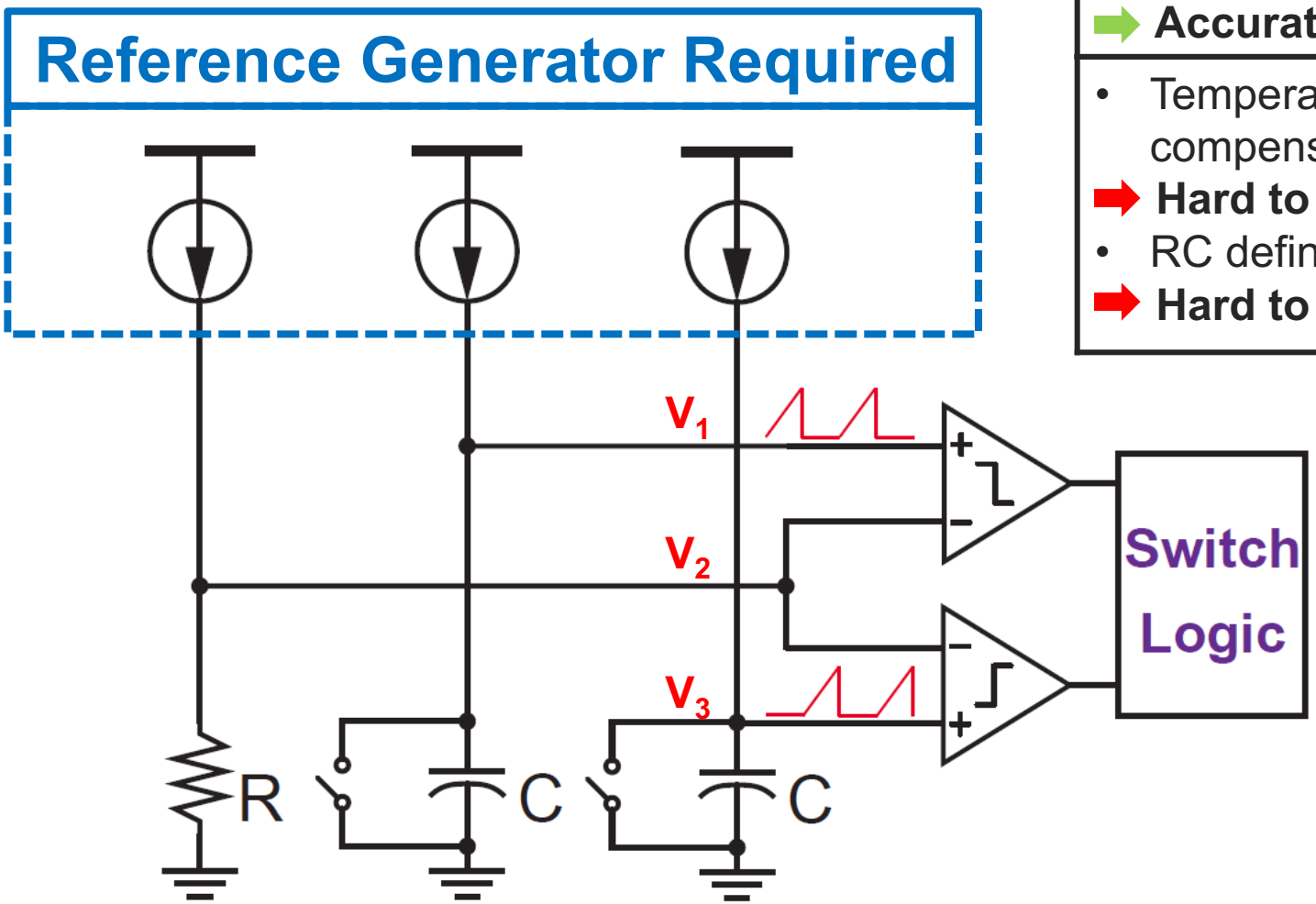
Ultra-Low-Power Timer with Low Supply Voltage

Outline

- On-Chip Oscillators
- Reference-Free Capacitive-Discharging Topology
- Frequency Stability, Area, Power
- Measurement Results
- Conclusions

Review: Relaxation Oscillator

- Basic Relaxation Oscillator



- Temperature stable voltages V_1, V_2, V_3
- ➡ **Accurate frequency**

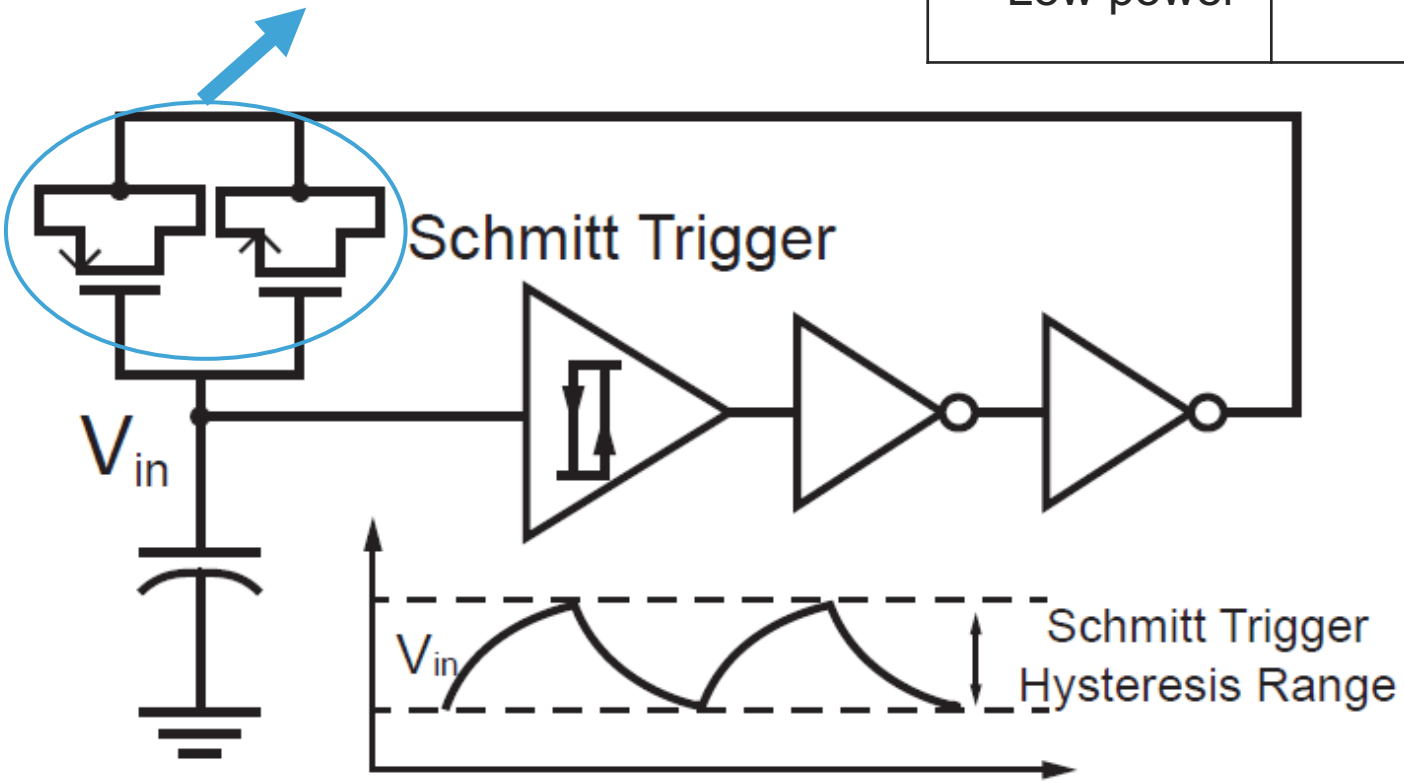
- Temperature compensated references
- ➡ **Hard to achieve pW**
- RC defines frequency
- ➡ **Hard to scale to Hz**

Review: One-Hot Topology

- Schmitt Trigger Based One-Hot Oscillator

Gate-Leakage as Current Reference

✓ Compact	➢ High temperature sensitivity
✓ Low power	

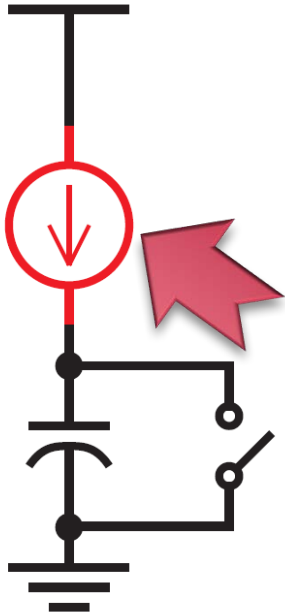


Lin, CICC 2007

Compared to Conventional Solutions

- Conventional oscillators

A ramp voltage is created by charging a capacitor with a temperature-stabilized current source



Hard to make it stable, low-current, and low-area for pW-level, Hz-range applications

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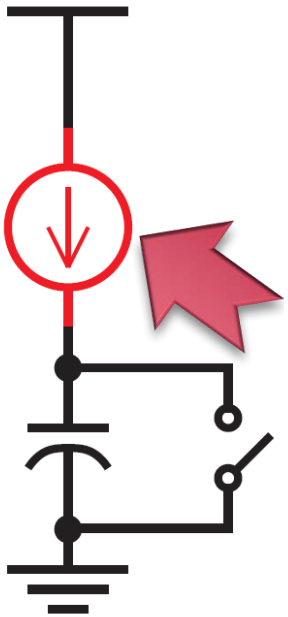
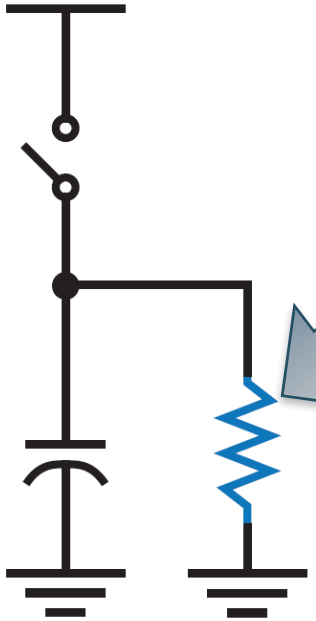


Hard to make it stable, low-current, and low-area for pW-level, Hz-range applications

- Proposed Architecture

A decaying voltage is obtained by discharging a pre-charged capacitor through a temperature-stable resistor

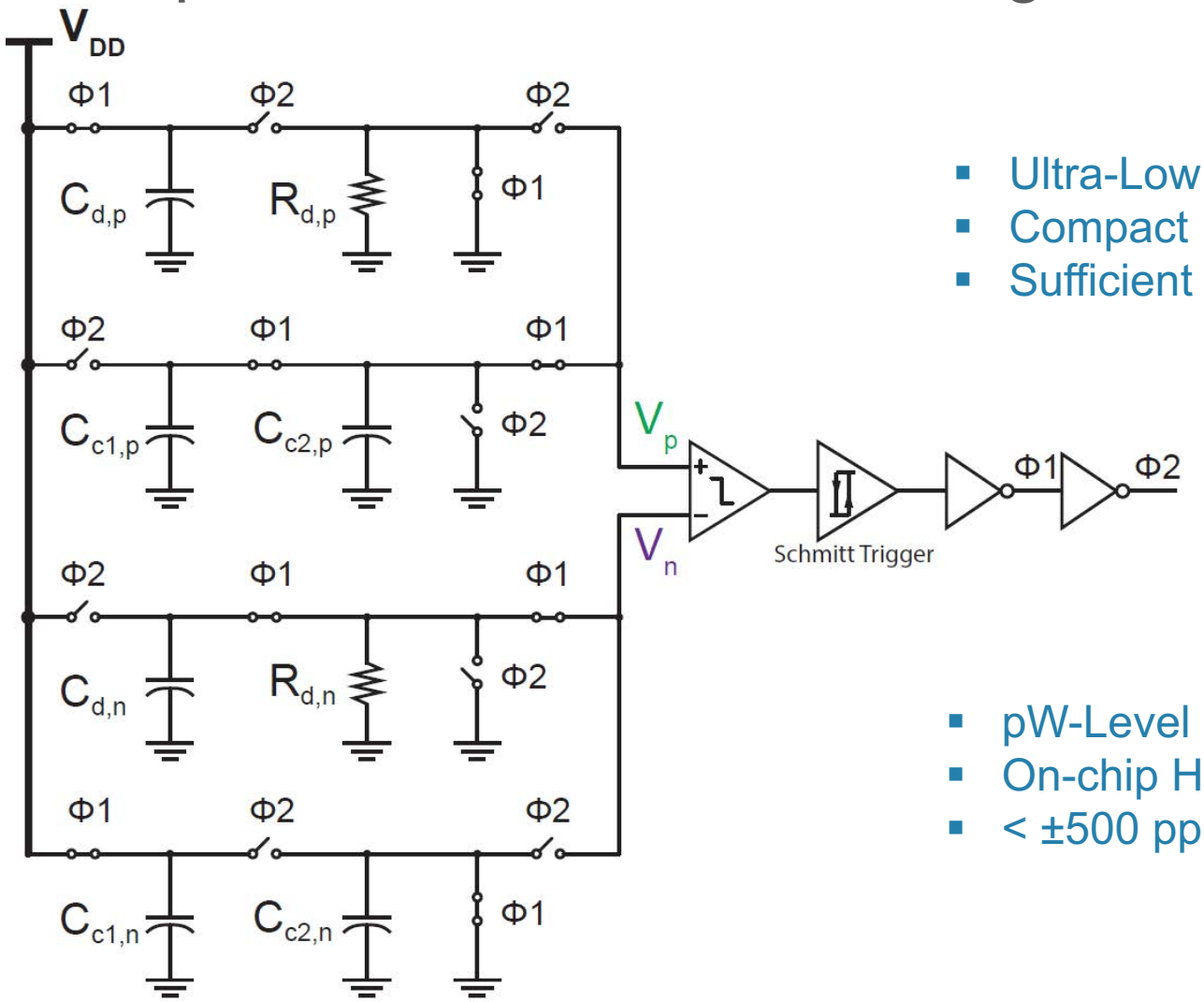


Easy to implement a low temperature-coefficient resistor, enabling stable, low-power, low-area solution

Proposed Architecture Provides a Low-Power, Low-Area, Low-Complexity Solution for Next-Generation Wireless Sensing Platforms

Reference-Free Capacitive-Discharging Topology

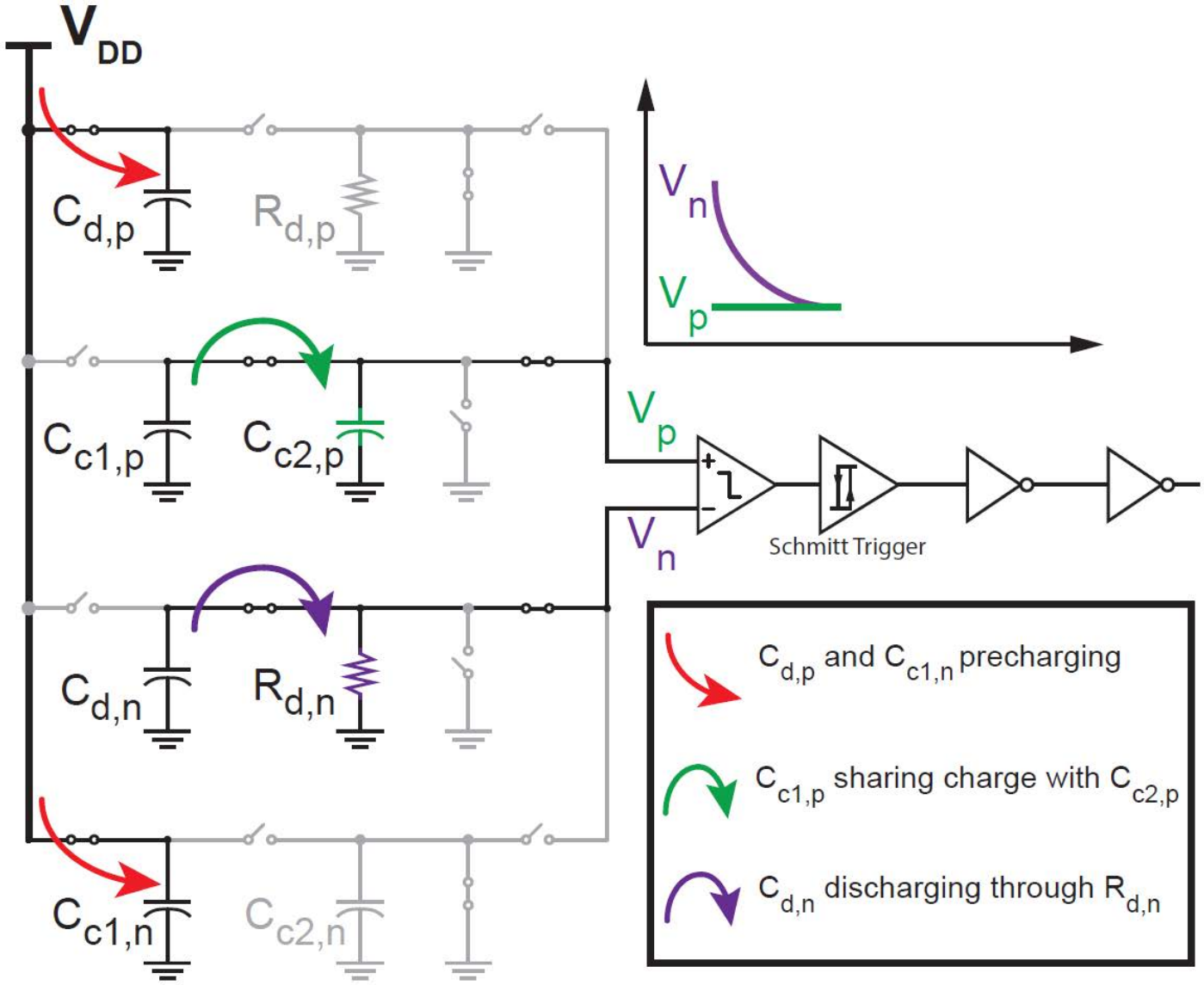
- Proposed Architecture and Target



- Ultra-Low Power
- Compact
- Sufficient Frequency Stability

- pW-Level power consumption
- On-chip Hz-range timer
- < ±500 ppm/°C

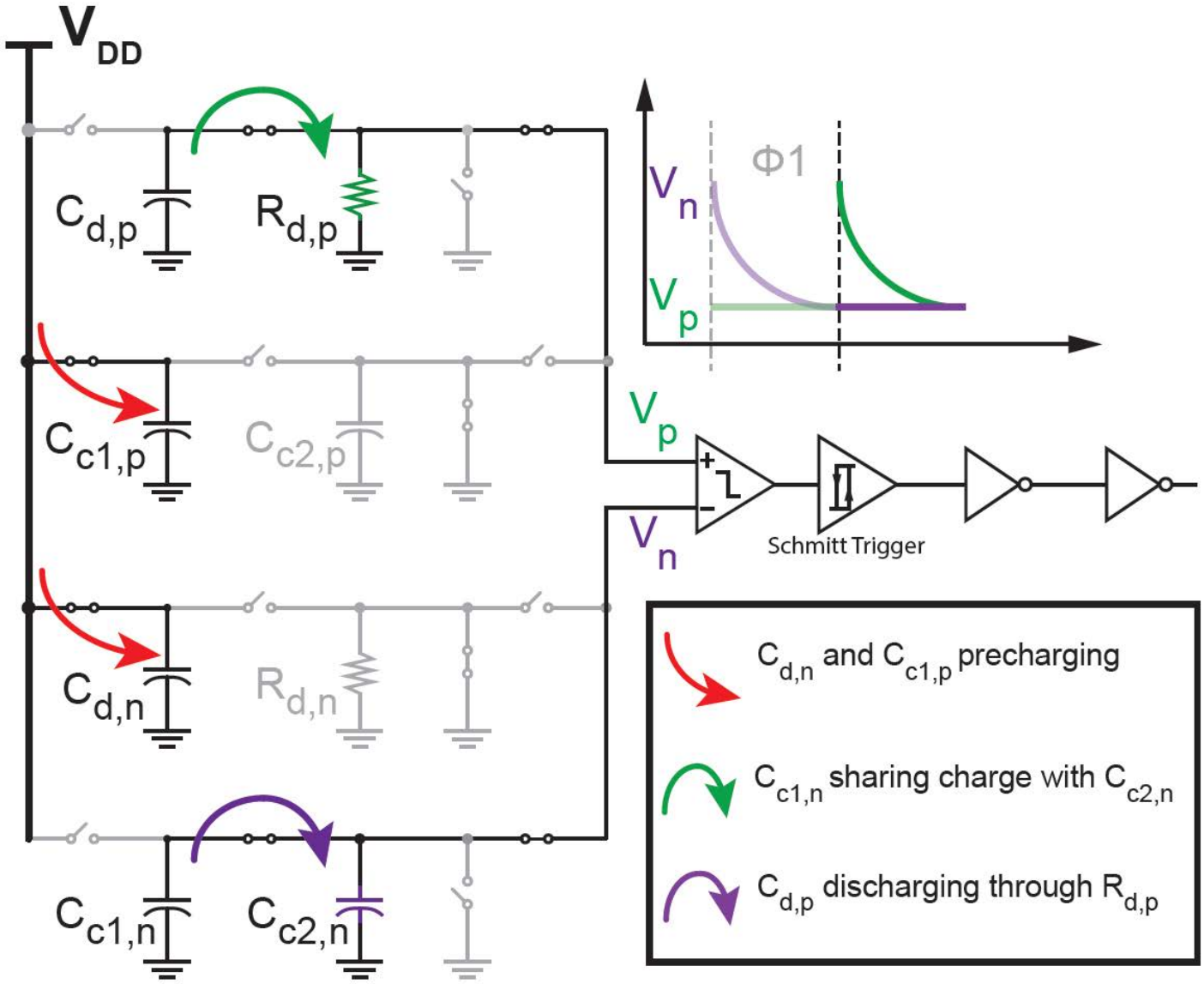
Oscillator Operation at Φ = 1



$$V_p = V_{DD}\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}$$

$$V_n = V_{DD}e^{-\frac{t}{R_{d,n}C_{d,n}}}$$

Oscillator Operation at Φ = 2



$$V_p - V_{DD}\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}$$

$$V_n - V_{DD}e^{-\frac{t}{R_{d,n}C_{d,n}}}$$

$$V_n = V_{DD}\frac{C_{c1,n}}{C_{c1,n}+C_{c2,n}}$$

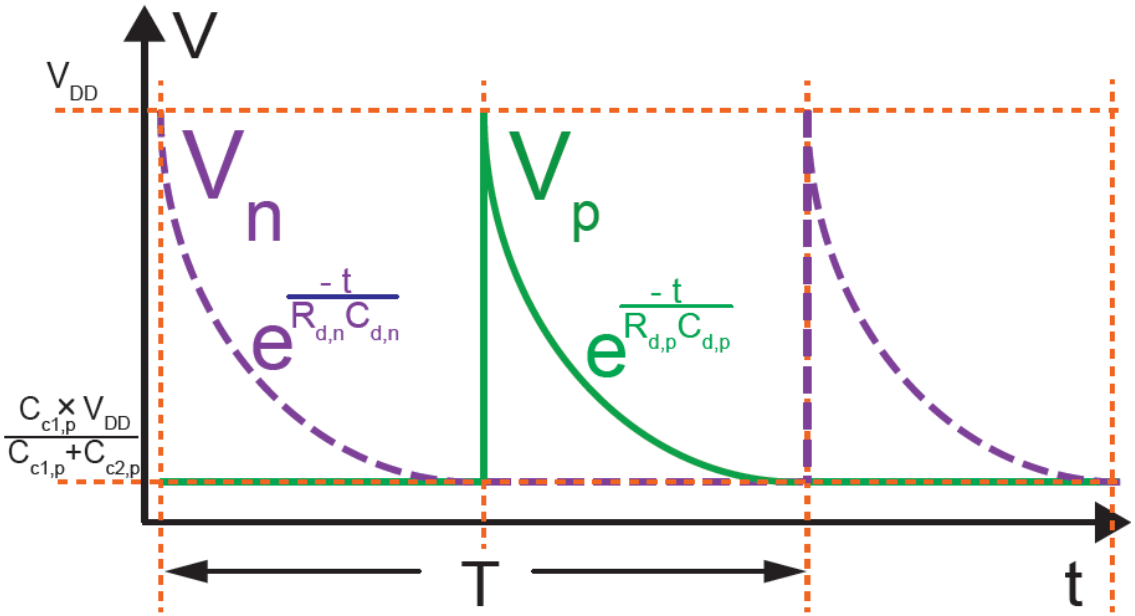
$$V_p = V_{DD}e^{-\frac{t}{R_{d,p}Cp}}$$

Frequency VS. Supply

$$T_{ideal} = 2R_{d,n}C_{d,n} \ln \frac{C_{c1,n} + C_{c2,n}}{C_{c1,n}}$$

No V_{DD} term in the equation
→ Rejected as common mode noise, by over 75 dB

- A reference voltage and a decaying voltage initialized from the same source
- Intrinsic relaxation-like operation ensures accurate frequency



To achieve 50% duty cycle
$C_{d,p} = C_{d,n}$; $R_{d,p} = R_{d,n}$; $C_{c1,p} = C_{c1,n}$; $C_{c2,p} = C_{c2,n}$

Frequency VS. Comparator Delay

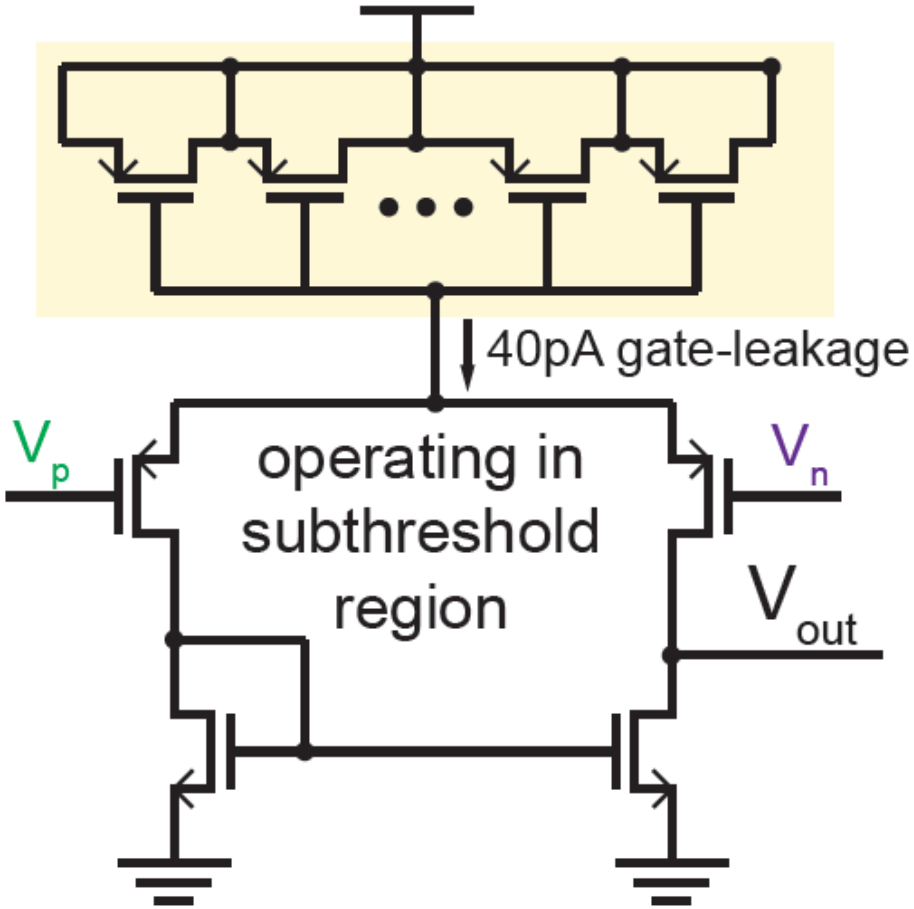
- Comparator delay varies w.r.t. temperature

  → **The variation in comparator delay impact oscillation frequency**

- **Comparator delay < 10 ppm of oscillation period**

→ The impact of comparator delay is minimized

- **Gate-leakage employed to bias comparator**



Frequency VS. Comparator Offset

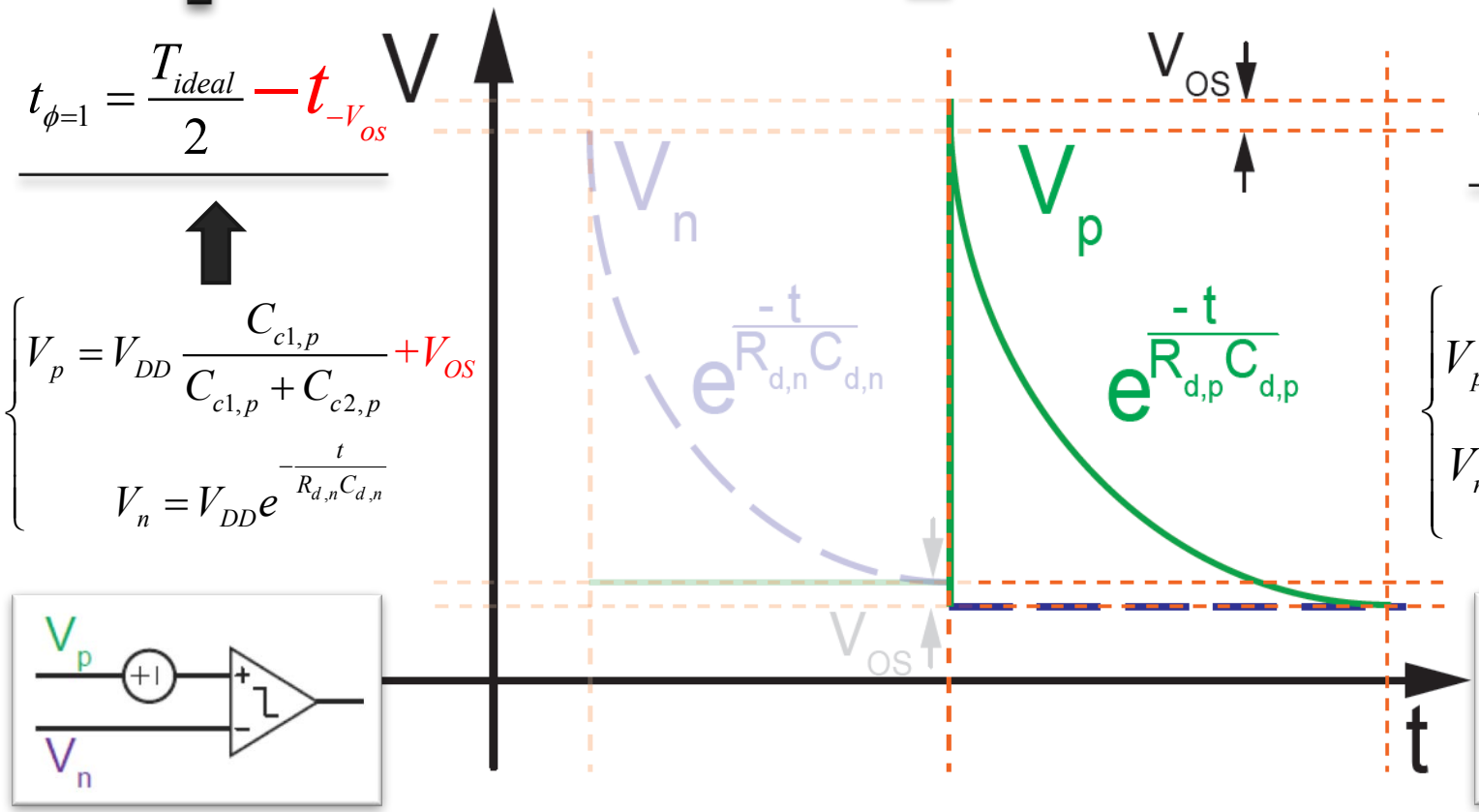
Offset is rejected through averaging, by over 25 dB

$$t_{osc} = T_{ideal} + (t_{+V_{os}} - t_{-V_{os}})$$

Small residue error exists due to exponential profile of the decaying voltage

$$t_{\phi=1} = \frac{T_{ideal}}{2} - t_{-V_{os}}$$

$$\begin{cases} V_p = V_{DD}\dfrac{C_{c1,p}}{C_{c1,p}+C_{c2,p}} + V_{OS} \\ V_n = V_{DD} e^{-\frac{t}{R_{d,n}C_{d,n}}} \end{cases}$$



$$t_{\phi=2} = \frac{T_{ideal}}{2} + t_{+V_{os}}$$

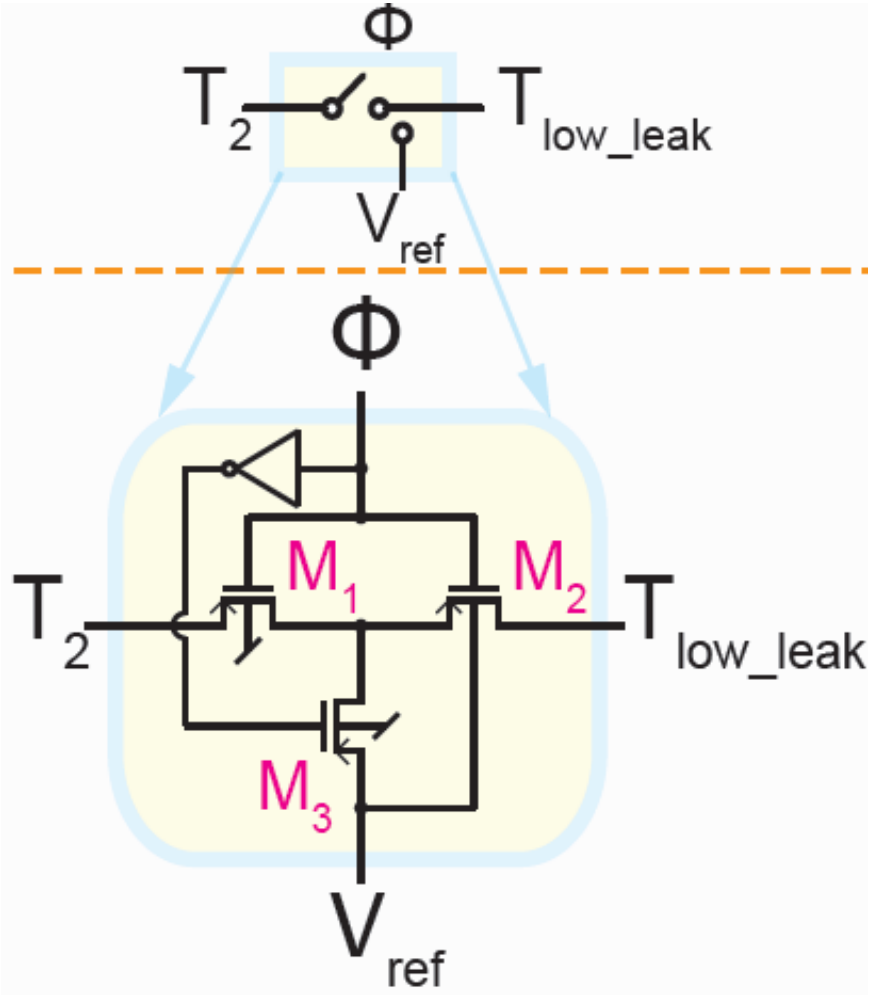
$$\begin{cases} V_p = V_{DD} e^{-\frac{t}{R_{d,n}C_{d,n}}} + V_{OS} \\ V_n = V_{DD}\dfrac{C_{c1,p}}{C_{c1,p}+C_{c2,p}} \end{cases}$$

Frequency VS. Switch Leakage

- Ultra-Low-Leakage Switch

- Oscillator operates at Hz-range
- Charge leakage can significantly impact oscillation frequency

Charge leakage is reduced by over 68 dB by employing ultra-low-leakage switch



O'Halloran, ISCAS2006

Area and Power Consumption

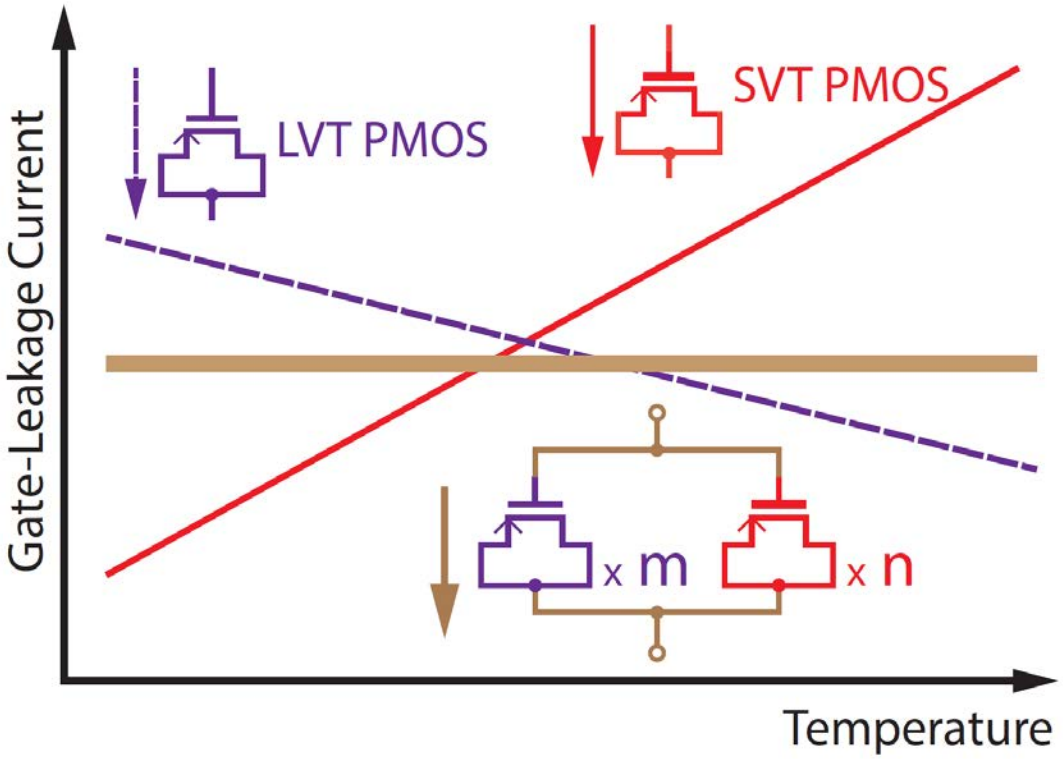
- Capacitors are sized to be 1.1 pF
  - Dynamic power due to the charging of capacitors is 27 pW
  - Moderate area consumption

$$T_{ideal} = 2R_{d,n}C_{d,n} \ln \frac{C_{c1,n} + C_{c2,n}}{C_{c1,n}}$$

- 300 GΩ Resistor for Hz-range
  - Too large for normal resistors

How to implement this resistor?

Implementing a large, temperature-stabilized resistance using gate-leakage devices



- Gate-leakage becomes prevalent as technology scales
- Employed to serve as resistor

- Temperature-Compensated Gate-Leakage

→ **Compact Design Achieved**

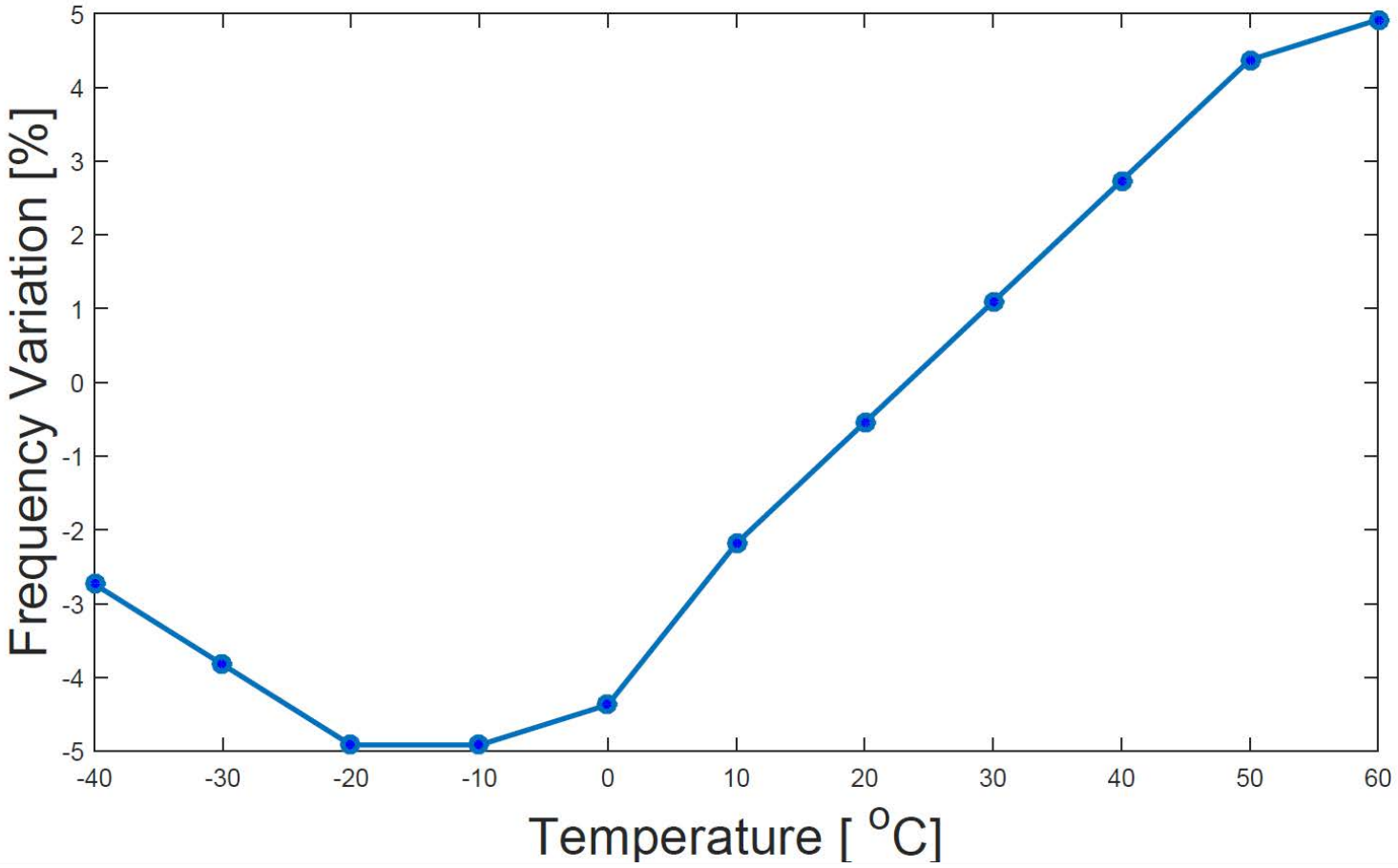
- Proposed Topology is Reference Free

→ **pW Power Consumption**

Dynamic Power	Comparator Power	Buffering Stages
27 pW	20 pW	4 pW

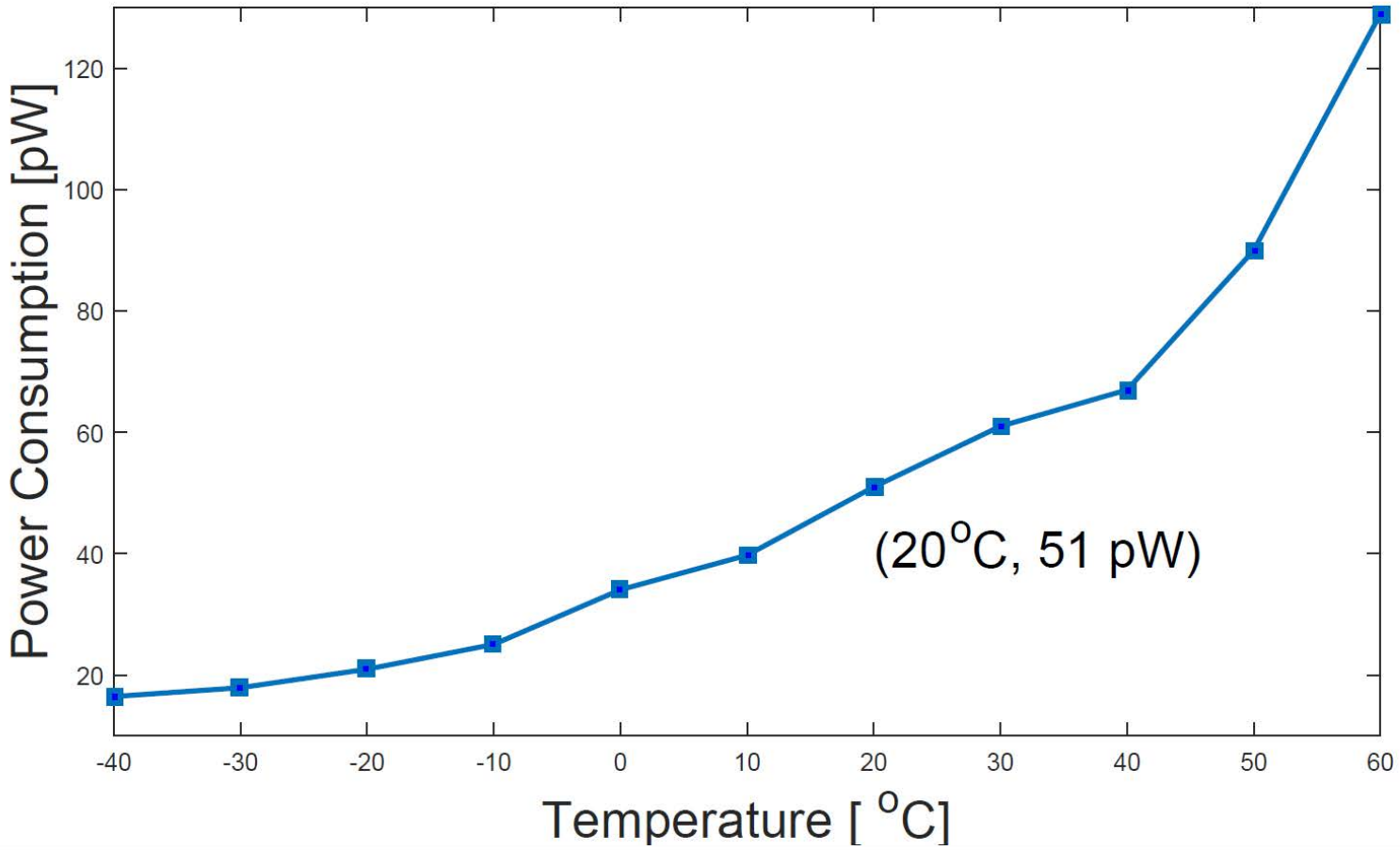
Lee, VLSI2000

Measured Frequency VS. Temperature



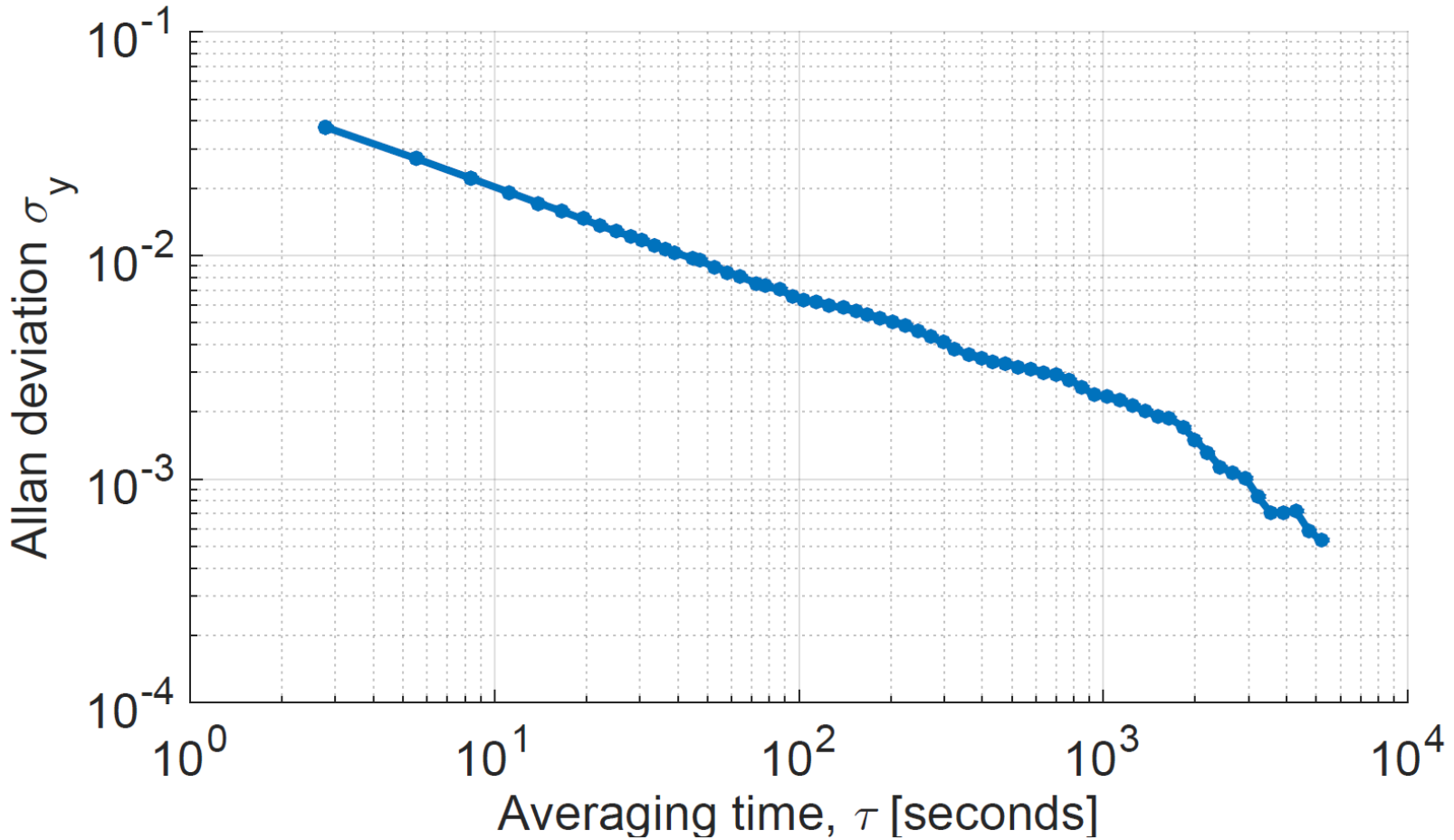
Across a temperature of -40 °C to 60 °C, the frequency deviates down to ±0.05%/°C

Measured Power VS. Temperature



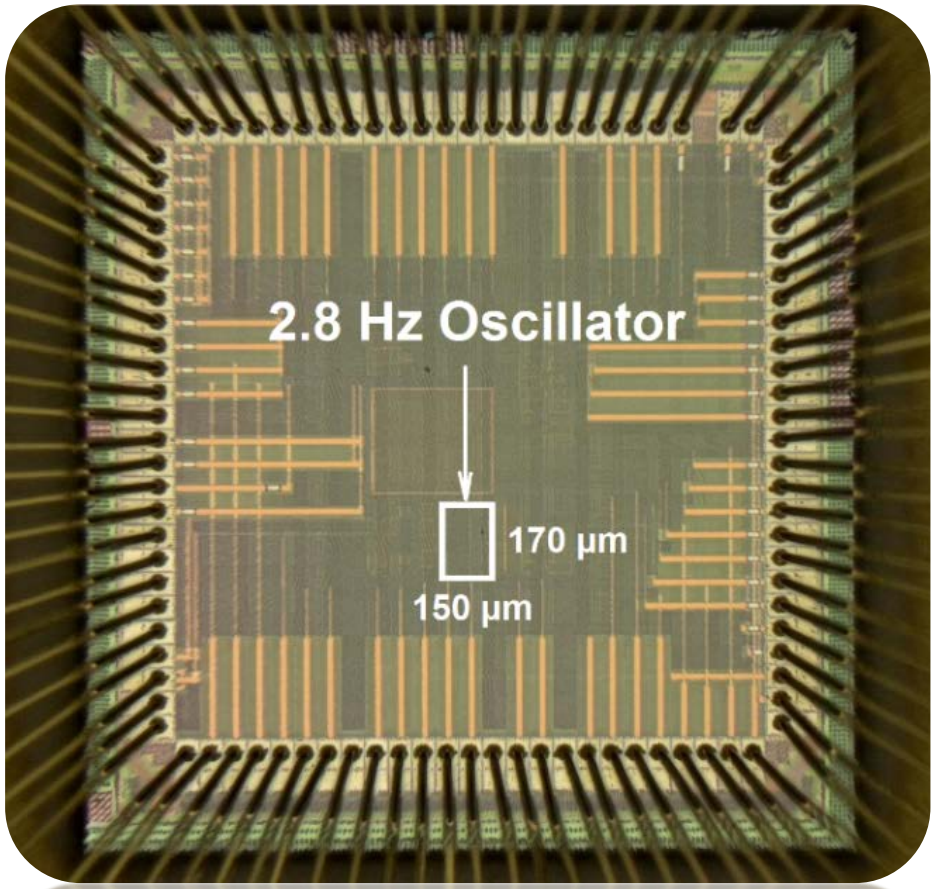
Consumes 51pW at 20 °C
-40 °C to 60 °C, consumes 16pW – 129pW

Measured Allan Deviation



Achieves an Allan deviation floor under 500 ppm at room temperature

Performance Summary



Process	**65 nm CMOS**
Area	**25500 µm^2**
Frequency	**2.8 Hz (nom.)**
Power	**51 pW**
Supply	**0.5 V**
Temperature Accuracy	**937 ppm/°C**
Temperature Range	**-40 °C to 60 °C**
Supply Sensitivity	**±1.9% @±10mV offset**
Allan Deviation Floor	**< 500 ppm**

Hz-Range Oscillator Comparison

Hz-Range Timers	[3] CICC'07	[2] ISSCC'09	[4] ISSCC'11	This Work	
Process	130 nm	130 nm	130 nm	**65 nm**	
Area [μm^2]	480	19,000	15,300[a]	**25,500**	
Frequency [Hz]	0.09	11.11	~ 5	**2.8**	
Power [pW]	120[b]	150[c]	660	**51**	
Temperature Accuracy [ppm/°C]	1600	490	31	**937**	
Temperature Range [°C]	0 to 80	0 to 90	-20 to 60	**-40 to 60**	
Supply Sensitivity	±7.5% @±50 mV Offset	+4%/-2% @±50 mV Offset	N/A	**±1.9%** @±10 mV Offset	**±3.5%** @±20 mV Offset
Allan Deviation Floor	N/A	N/A	N/A	**< 500 ppm**	

[a] The area of the Timer and Controller is 10,500 μm^2 and 4,800 μm^2, respectively.
[b] Operates at 450 mV.
[c] 100 pW when refreshed every 4 minutes.

Conclusion

- Reference-free capacitive-discharging structure ensures pW-level power consumption
- Intrinsic relaxation-like operation enables accurate frequency
  - Comparator offset cancellation through averaging
- Temperature-compensated gate-leakage as resistor ensures small area for Hz-range oscillator

Acknowledgement

- STMicroelectronics for chip fabrication

A 51 pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8 Hz

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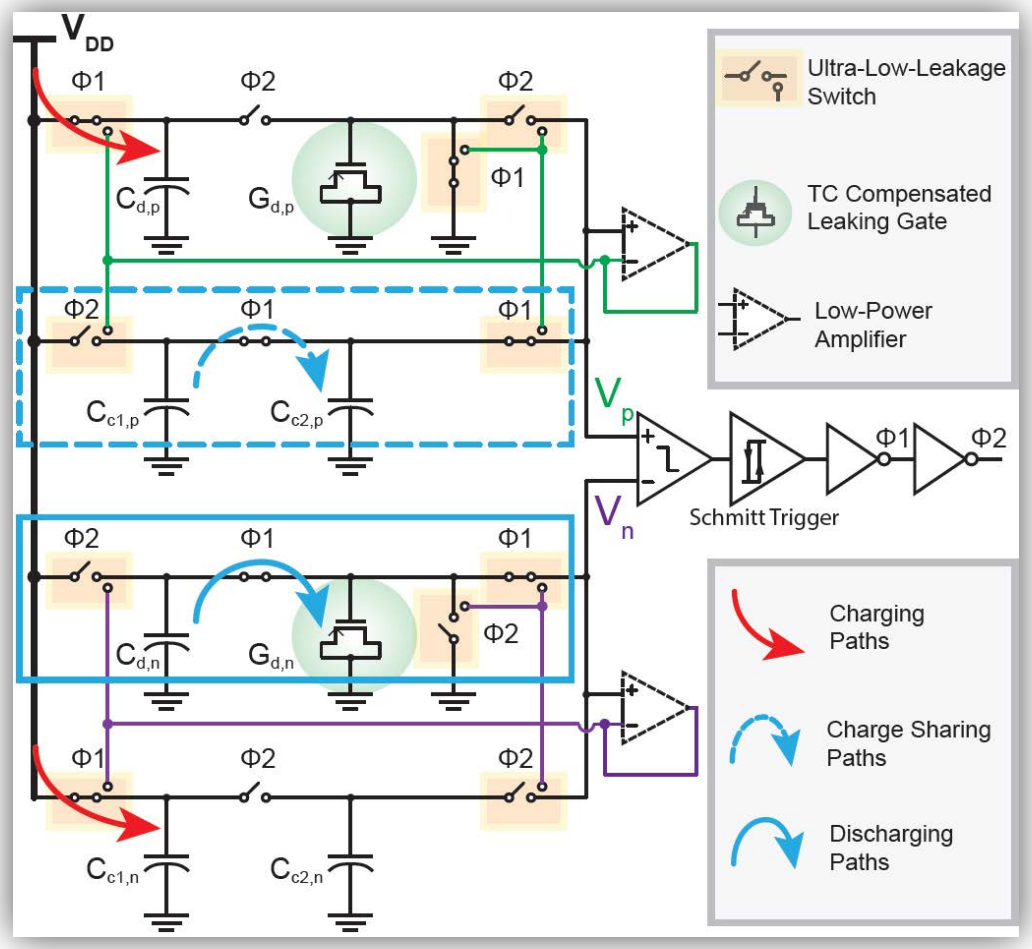

Questions