A Footprint-Constrained Efficiency Roadmap for on-Chip Switched-Capacitor DC-DC Converters

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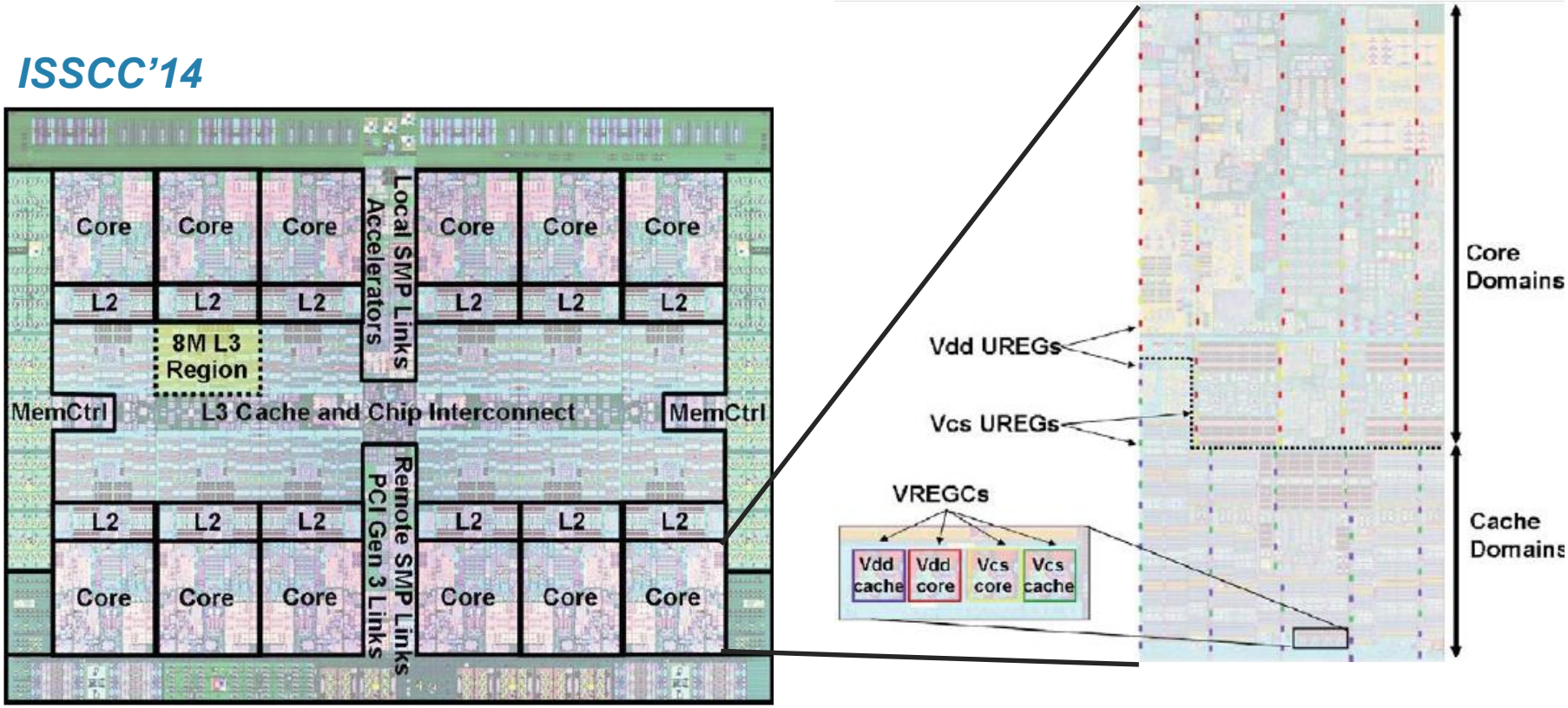
Voltage domain challenges in modern SoCs

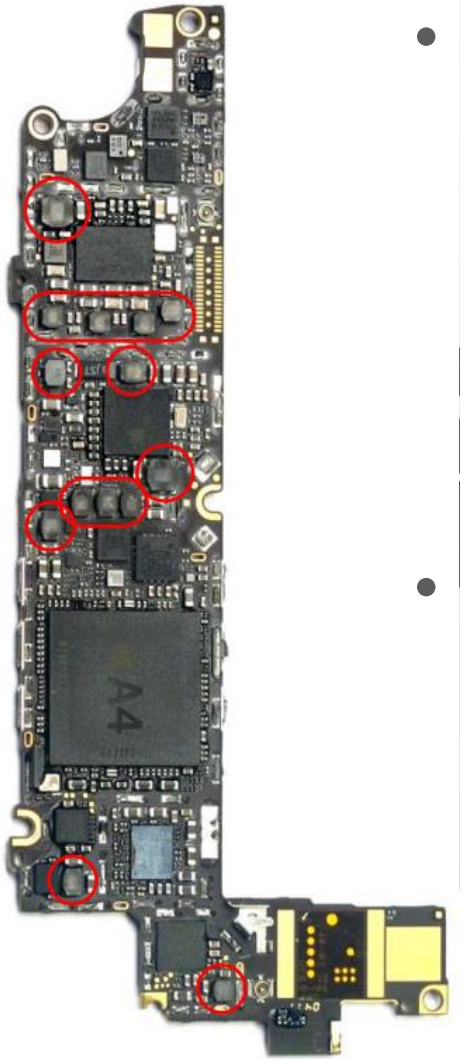
Example: IBM POWER8

ISSCC'14



Challenge: powering 48 independent dynamic voltage and frequency scaling (DVFS) domains

Powering multiple domains

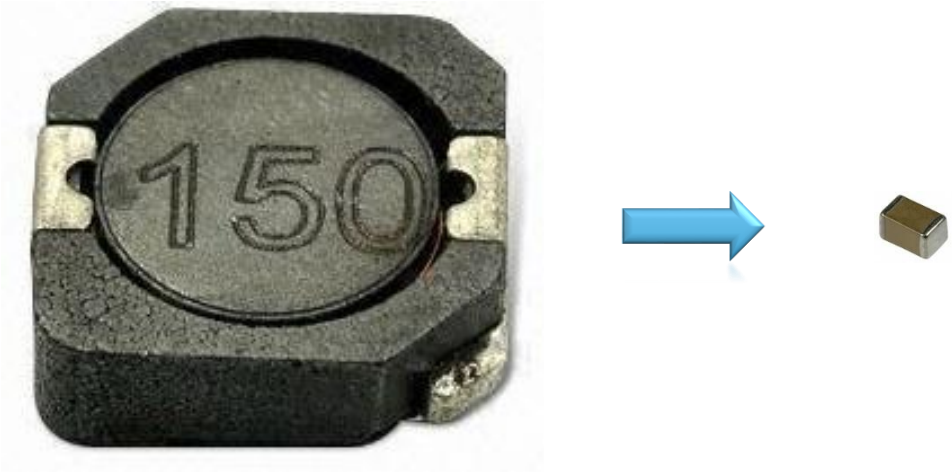


Source: Sunlord Inc.

- Solution 1: inductive converters
  - PROS:
    - High efficiency
    - Large Vin-Vout range possible
  - CONS:
    - Inductors are large & do not scale
- Solution 2: linear regulators
  - PROS:
    - Very small, can fully integrated into SoC
    - Stable, low-noise
  - CONS:
    - Efficiency < Vout/Vin; can be very small at large voltage conversion ratios

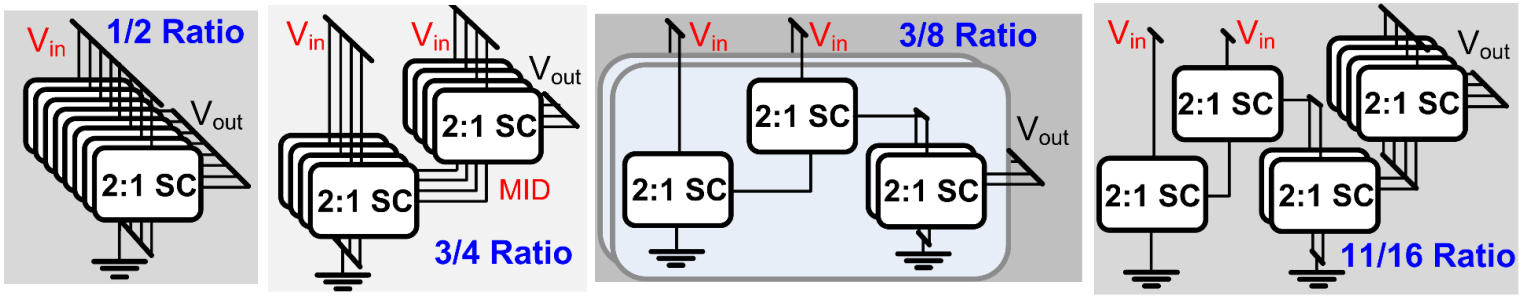
Switched-capacitor DC-DC converter: inherent size advantage

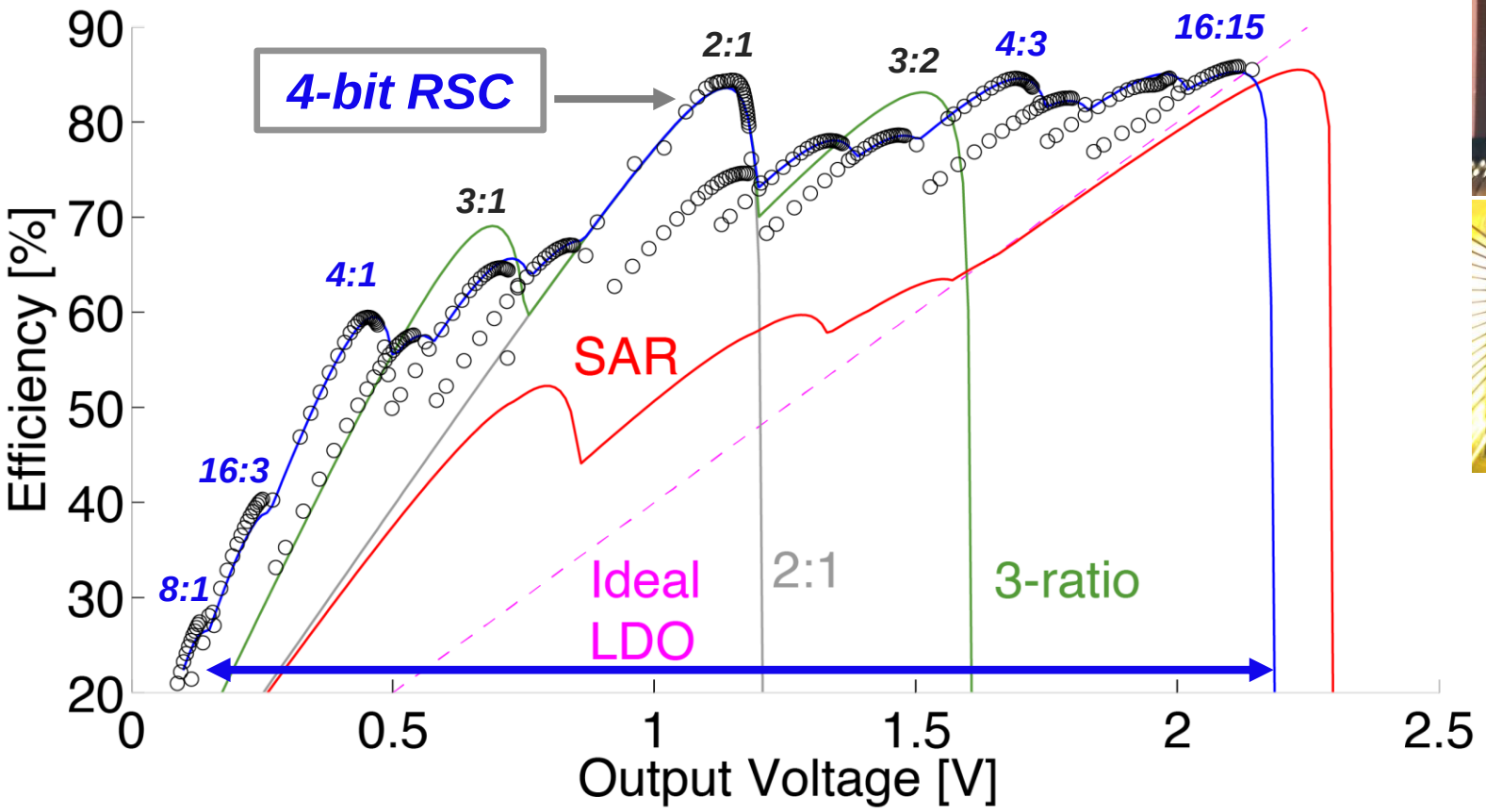
- Solution 3: switched-capacitor converters

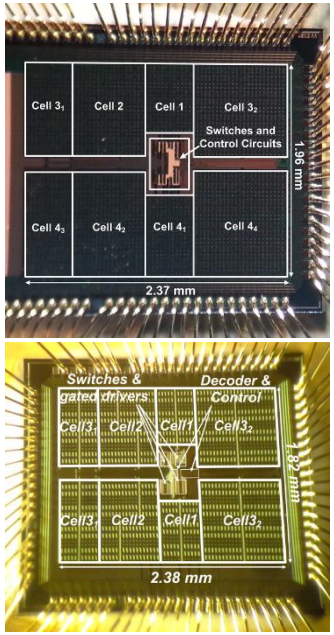


  - PROS:
    - Higher inherent power and energy density than inductors
    - Easily integrated on-chip (e.g., MIM, MOSCAP, DT, etc.)
    - Can leverage existing on-chip decoupling
  - CONS:
    - Prior-art has limited output voltage range (limited by discrete conversion ratios)

Solving the output voltage problem via recursive switched capacitor topologies

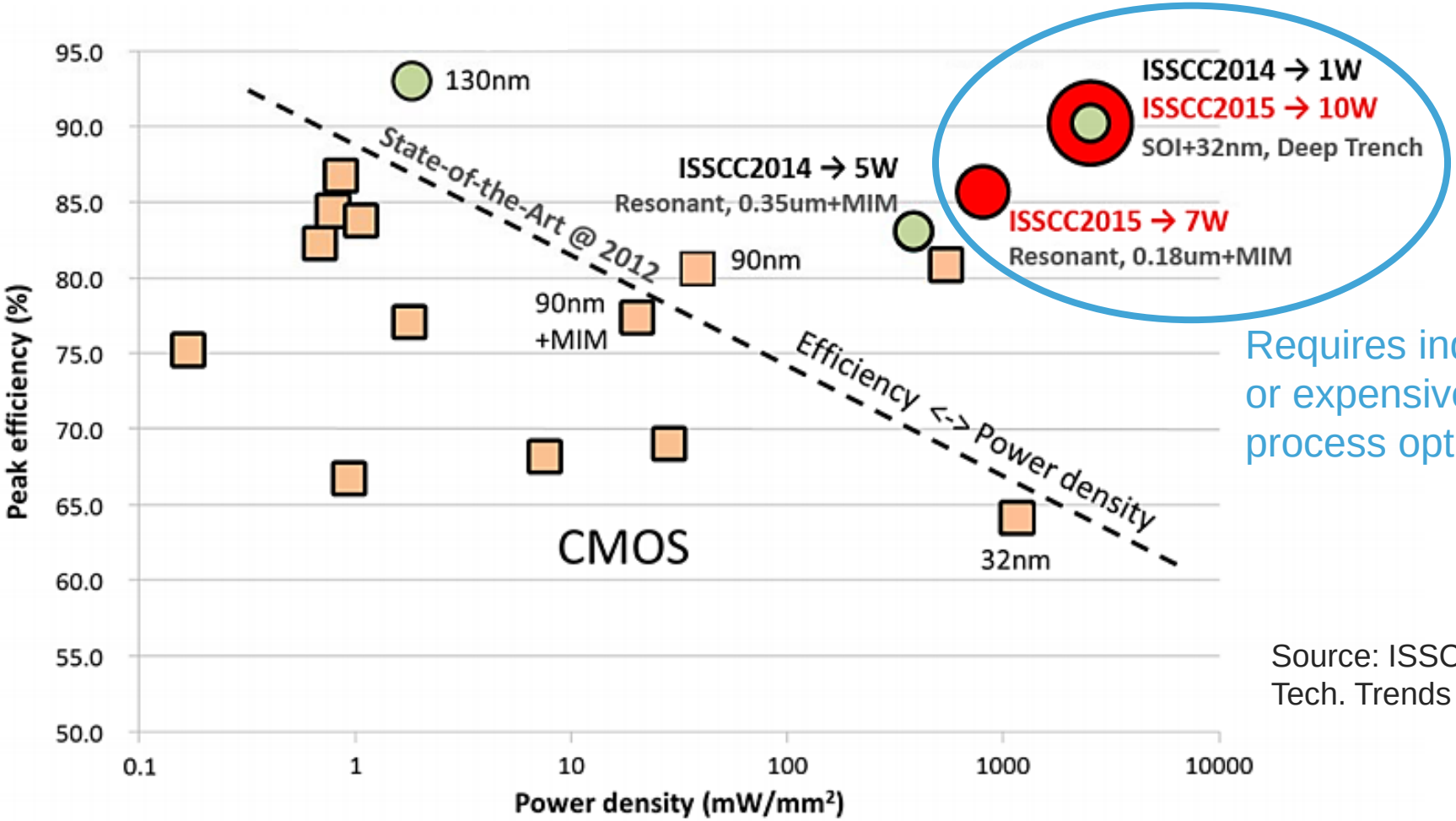






[Salem & Mercier, ISSCC, CICC, JSSC 2014]

Switched Capacitor power density

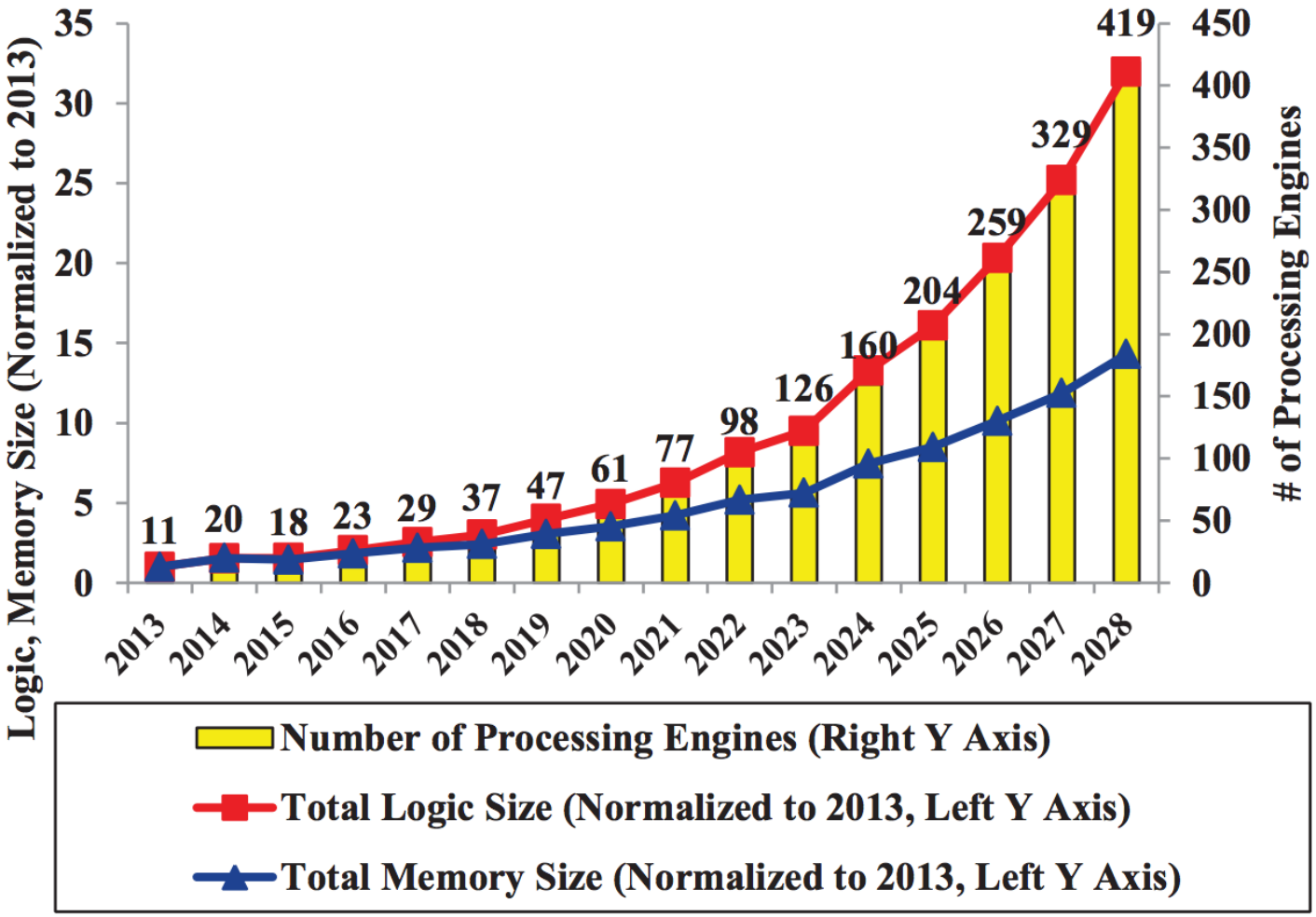


Requires inductors or expensive process options

Source: ISSCC Tech. Trends

Power density and efficiency are improving. How much do we need moving forward?

Using the *International Technology Roadmap for Semiconductors (ITRS)* as a guideline

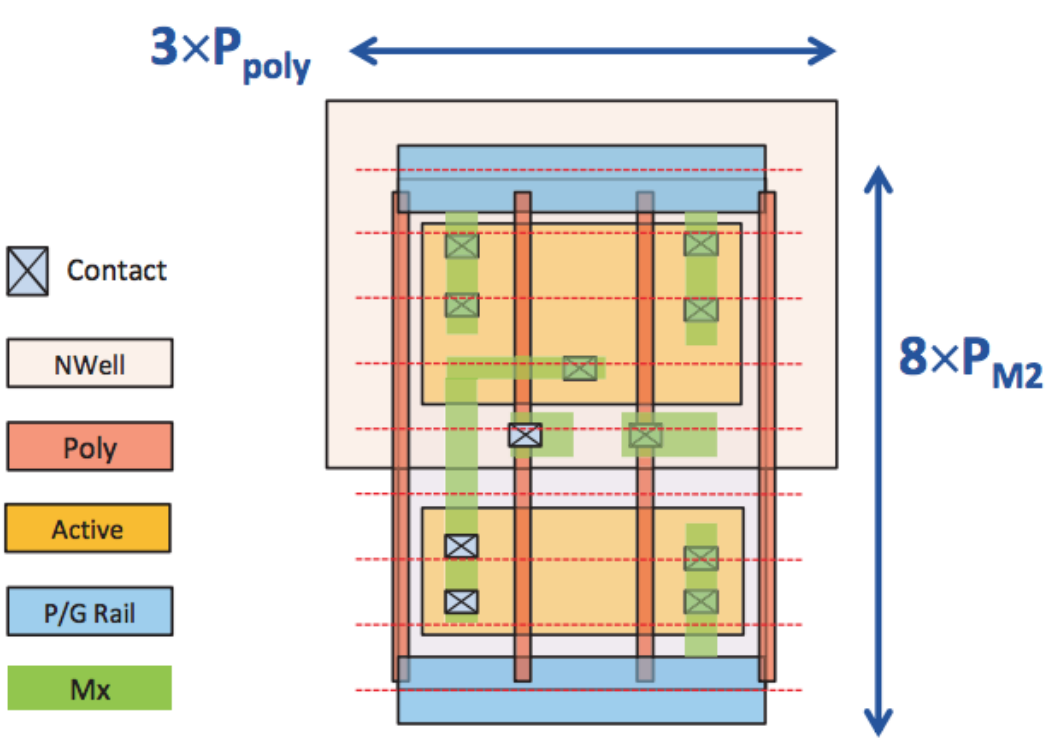


This work: focus on consumer-portable SoCs (SoC-CP*)

* Using 2011 numbers, since the 2013 SoC-CP chapter is not currently available online

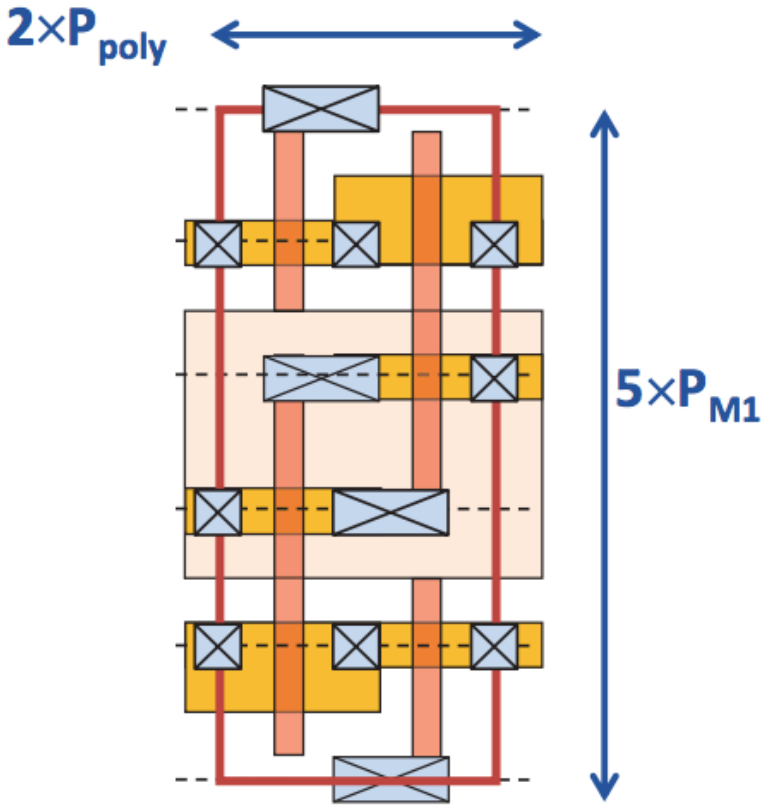
ITRS canonical cell area

Define *F* = Metal 1 half-pitch



$U_{logic} = 3P_{poly} \times 8P_{M2} = 180F^2$

calibrated → $175F^2$



$U_{SRAM} = 2P_{poly} \times 5P_{M1} = 60F^2$

Computing cell area and power density

- *ITRS*: logic and memory area can be represented by canonical cells (NAND2, SRAM) with overhead factors: $O_{logic} = 2.0,\ O_{SRAM} = 1.6$

Logic

$$D_{tr,logic} = \frac{4}{O_{logic} U_{logic}}$$

Transistor density

Trans. unit cap.

Wiring cap.

$$D_{cap,logic} = D_{tr,logic} C_g W_{logic} + D_{l,eff} C_w$$

$$P_{dynamic,logic} = \alpha_{logic} \left(\beta + \frac{1}{3}(1-\beta) \right) D_{cap,logic} f_c V_{DD}^2$$

Not all nodes on critical path – lower activity

SRAM

$$D_{tr,SRAM} = \frac{6}{O_{SRAM} U_{SRAM}}$$

Transistor density

Cap. per SRAM trans.

$$P_{dynamic,SRAM} = \alpha_{SRAM} D_{tr,SRAM} 2 C_g W_{SRAM} f_c V_{DD}^2$$

P_{static}: Logic & SRAM

Half of all branches leak

$$P_{static} = \frac{1}{2} D_{tr} I_{off} V_{DD}$$

Putting the model together

- To accommodate low-power design techniques such as DVFS, power gating, body biasing, etc., ITRS includes a power improvement factor, γ

$$P_{logic,total} = \frac{P_{dyn,logic}}{\gamma_{dyn}} + \frac{P_{static,logic}}{\gamma_{static}}$$

$$P_{SRAM,total} = \frac{P_{dyn,SRAM}}{\gamma_{dyn,SRAM}} + \frac{P_{static,SRAM}}{\gamma_{static,SRAM}}$$

$$P_{chip,total} = \frac{S_{logic}P_{logic,total} + S_{SRAM}P_{SRAM,total}}{S_{logic} + S_{SRAM}}$$

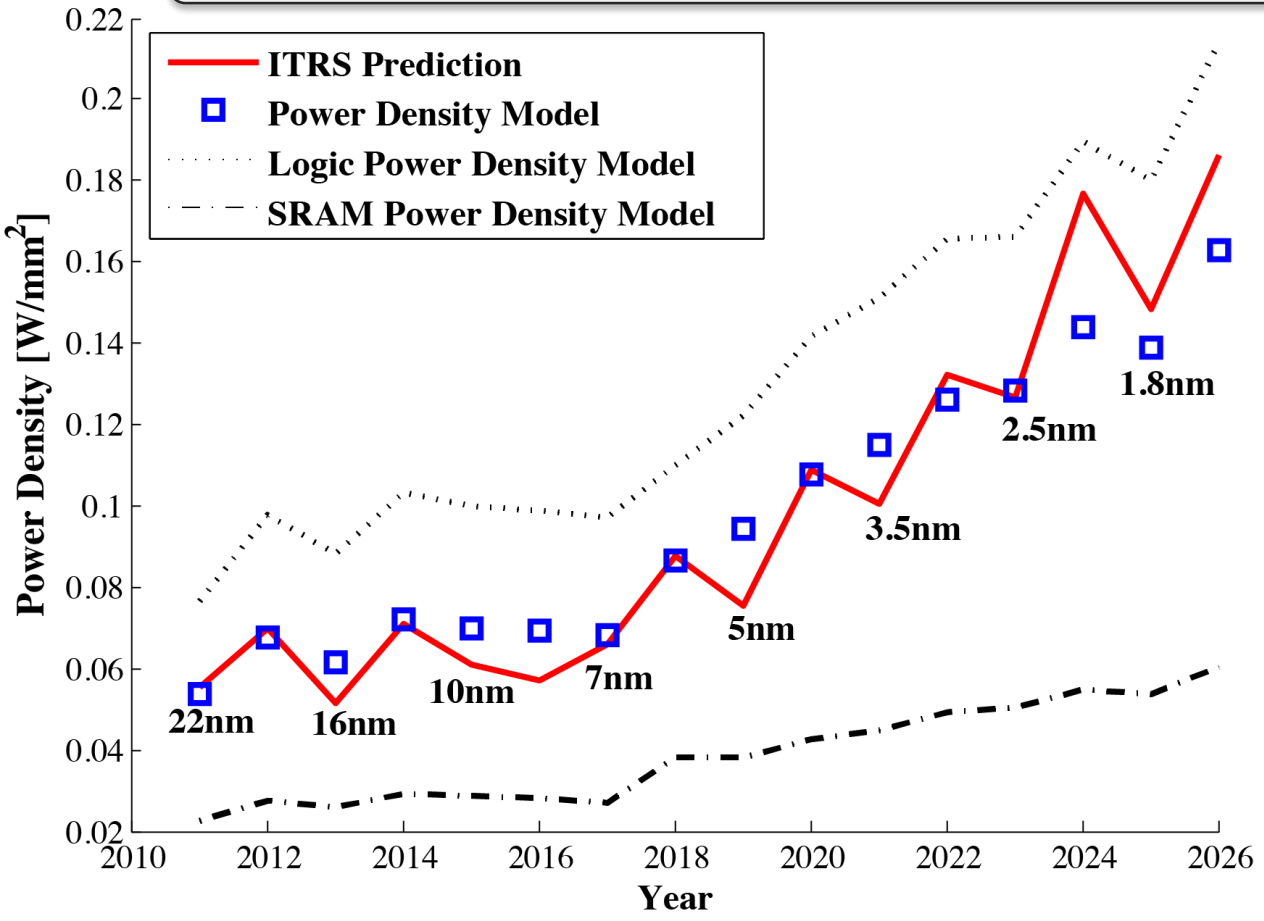
Total area: $O_{logic}U_{logic}N_{gates}$ $O_{SRAM}U_{SRAM}N_{bits}$

- N_{gates} and N_{bits} found under ITRS System Drivers chapter
- Assume 250kGate / 1Mbit ratio between logic and memory

Model results

- Input to model from ITRS process integration, devices, and structures (PIDS) chapter

$$F, \quad C_g, \quad I_{off}, \quad D_l, \quad C_w, \quad V_{DD}, \quad \gamma, \quad f_c$$

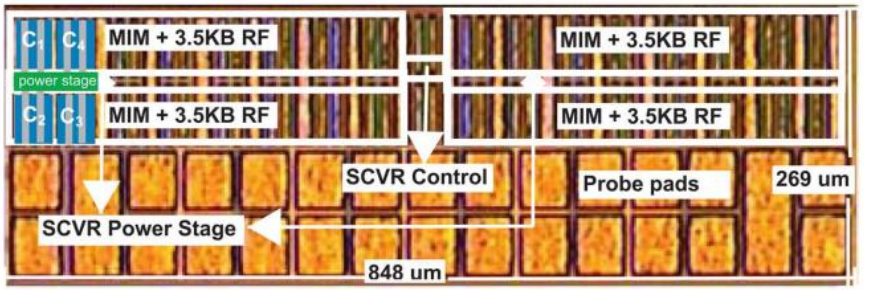


Developed model matches ITRS results to within 15%.

Importantly, breaks out power density of logic and SRAM

Exploiting decoupling capacitance for integrated SC conversion

- All DC-DC converters, including integrated LDOs, use decoupling capacitance
- Recent work is exploiting this for SC conversion without additional area overhead



[R. Jain et al., JSSC 2014]

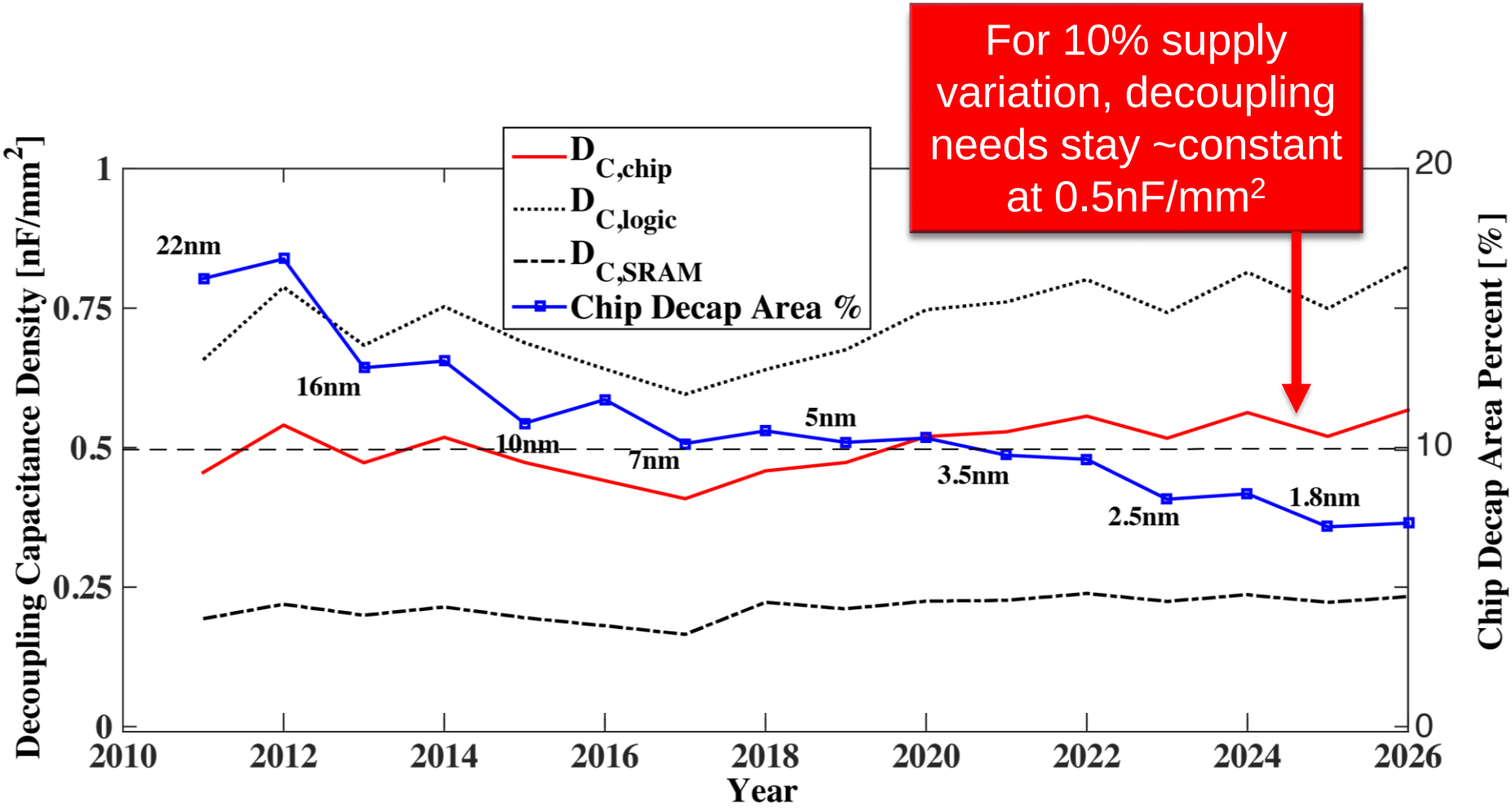
- Optimal amount of decoupling to suppress noise [11]:
  - $C_{decap} = \frac{I}{2nf_cV_{DD}}$

Tolerated fractional supply noise

- Assuming C_{decap} is included in O_{logic}, O_{SRAM}, decap density can be found as:
  - $D_{decap,logic|SRAM} = \frac{P_{total,logic|SRAM}C_{decap}}{V_{DD}I} = \frac{P_{total,logic|SRAM}}{2nf_cV_{DD}^2}$

[11] M. Pant, P. Pant, and D. Wills, "On-chip decoupling capacitor optimization using architectural level prediction," Trans. on VLSI, vol. 10, no. 3, pp. 319–326, Jun. 2002.

Scaling decoupling capacitor requirements



A footprint-constrained SC roadmap: efficiency

- 2:1 SC losses can be summarized by: [4]

$$\frac{P_{loss}}{P_L} = 3\sqrt[3]{2\frac{I_L}{D_{cap}}\frac{R_{on}C_g}{V_{DD}}}$$

Current density

Switch resistance and capacitance

Capacitance density

- Recall that $\frac{I_L}{D_{cap}} = 2nf_cV_{DD}$, and thus:

$\tau = R_{on}C_g$ (intrinsic transistor delay)

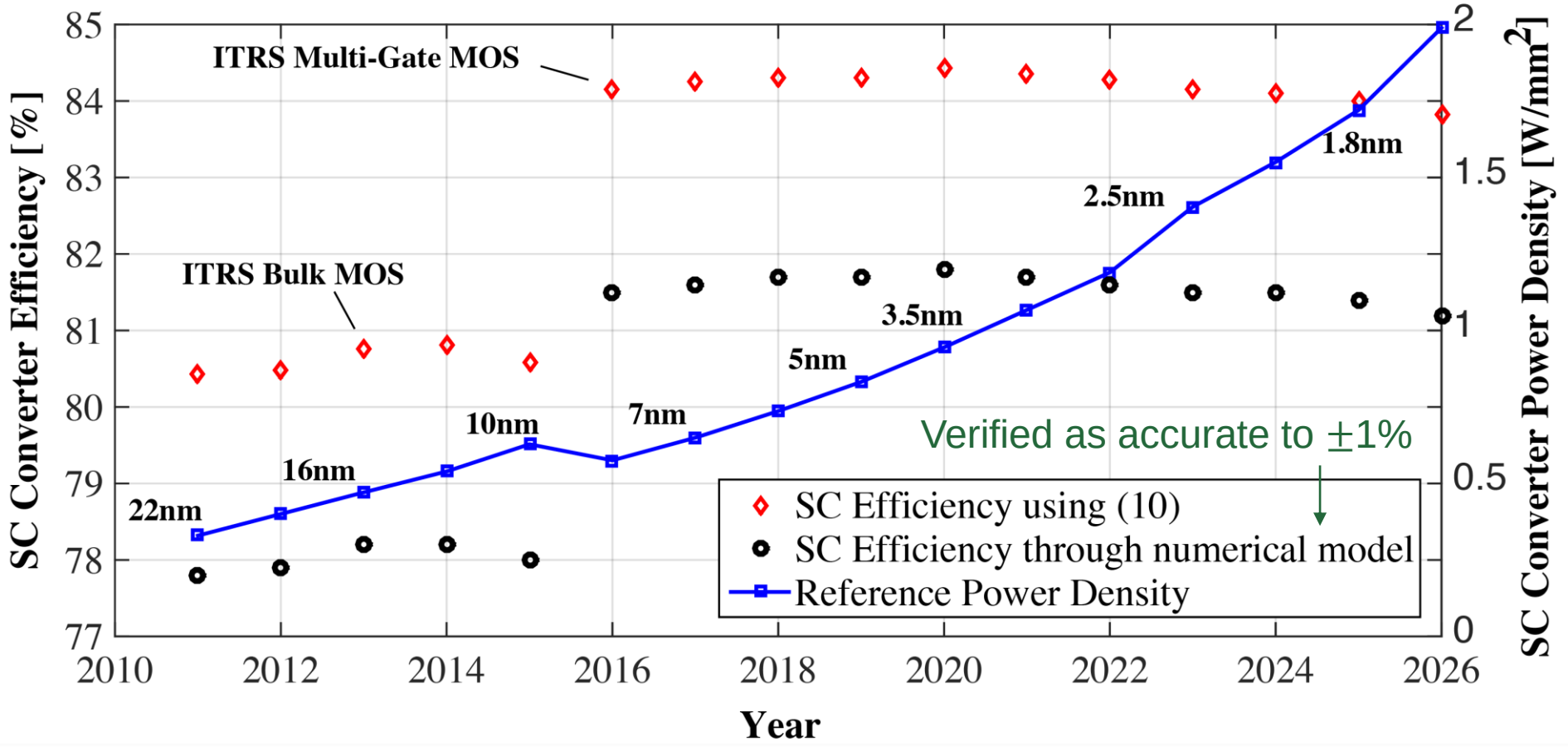
$$\frac{P_{loss}}{P_L} = 3\sqrt[3]{4nf_c\tau}$$

Losses of SC converter using on-chip decoupling capacitance

↳ Depends on frequency-transistor delay product

[4] L.G. Salem, P.P. Mercier, "A Recursive Switched-Capacitor DC-DC Converter Achieving 2^N-1 Ratios With High Efficiency Over a Wide Output Voltage Range," *IEEE Journal of Solid-State Circuits (JSSC)*, Dec. 2014.

A footprint-constrained SC roadmap: results



Constraining ourselves to only using area required for decoupling in future nodes, achievable power density increases with scaling, and efficiency is > 80%

Conclusions

- Switched capacitor DC-DC converters offer both high-efficiency and small size
  - Output voltage ranges are getting better
- Recent work has shown ultra-high power density is achievable, yet requires:
  - Inductors
  - Expensive process options
- This work presented a model describing the achievable efficiency and power density of SC converters with no area penalty by using on-chip decoupling
- 0.5W/mm^2 is sufficient in current-generation technologies, 1-2W/mm^2 easily achievable in future technologies using only MOS capacitors
- Deep-trench or resonant converters may not be necessary to meet the demands of current and future SoC-CP applications