A Flying-Domain DC-DC Converter Powering a Cortex-M0 Processor with 90.8% Efficiency

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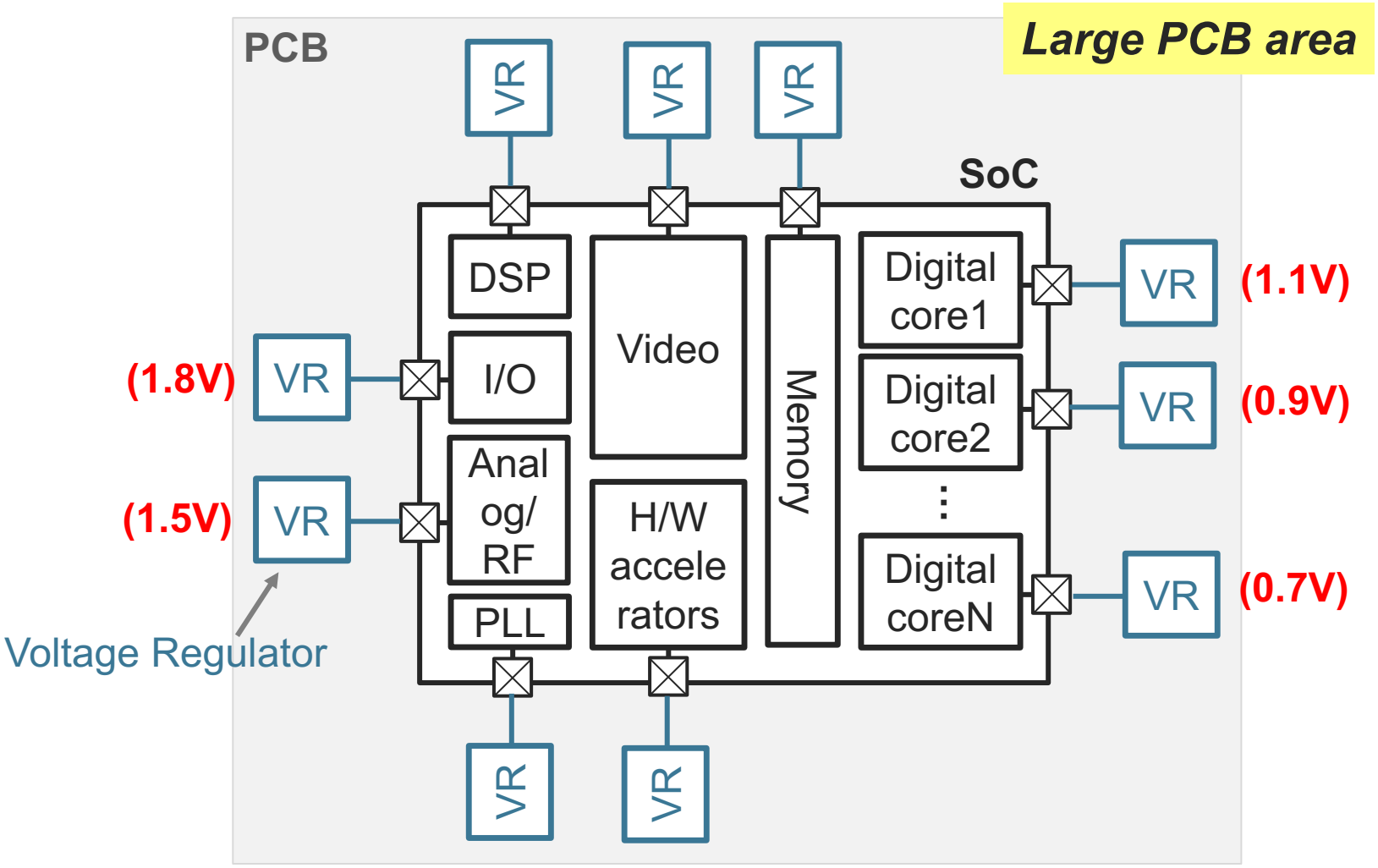
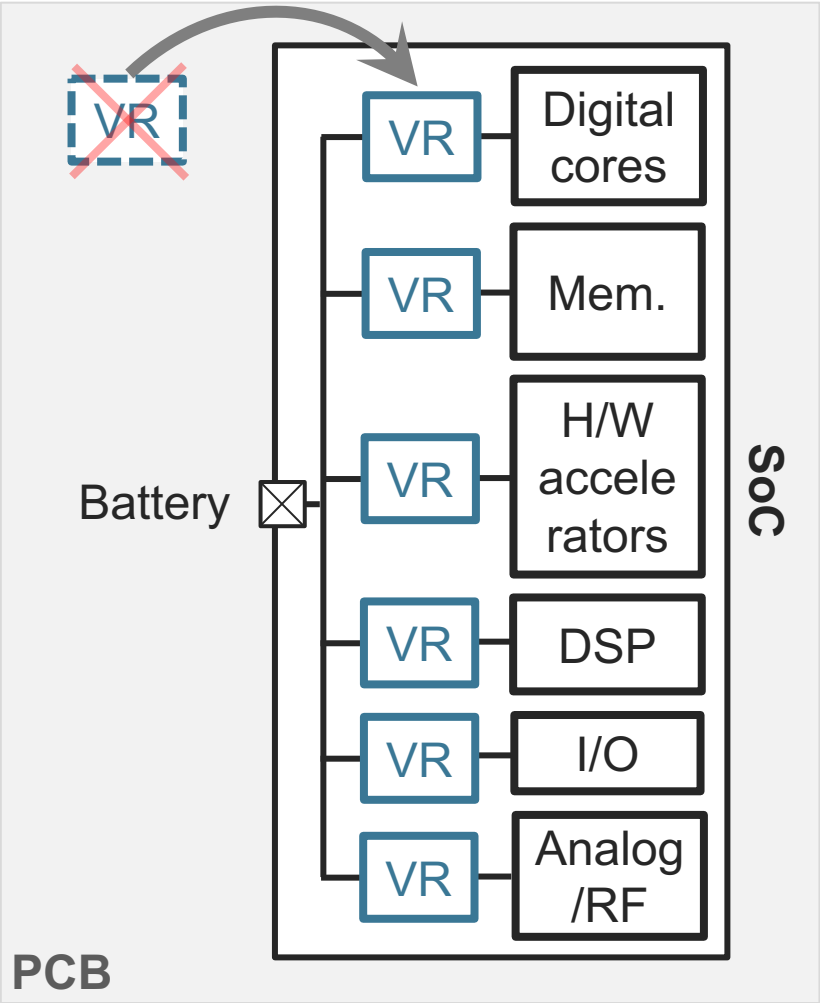
On-Chip Voltage Regulators are Essential

- Independent supply for each module for per-block power management



On-Chip Voltage Regulators are Essential

- **Bring the off-chip VRs into the chip for lower cost**



- Lower PCB area & product form-factor
- Lower BOM & I/O number

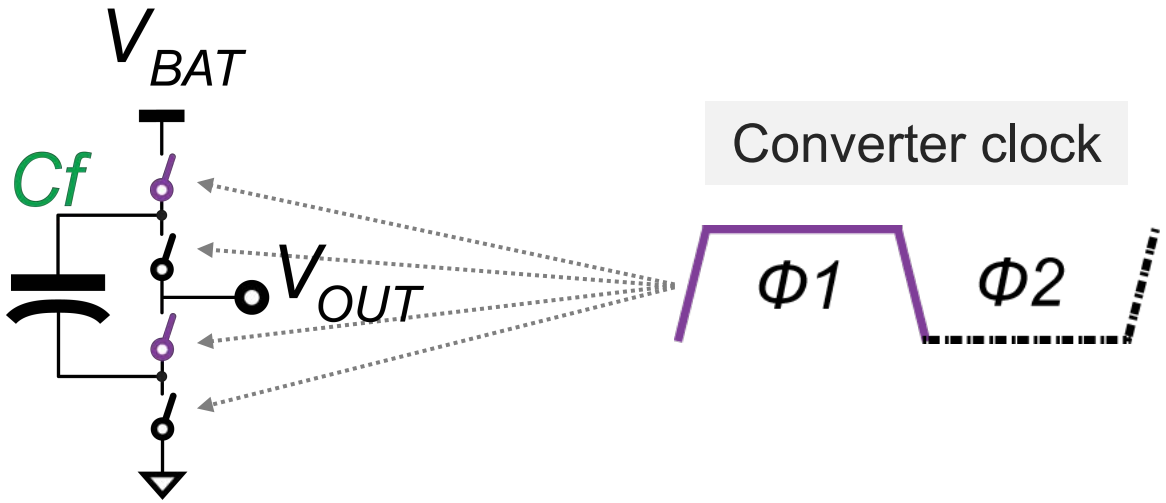
Requires high density converters

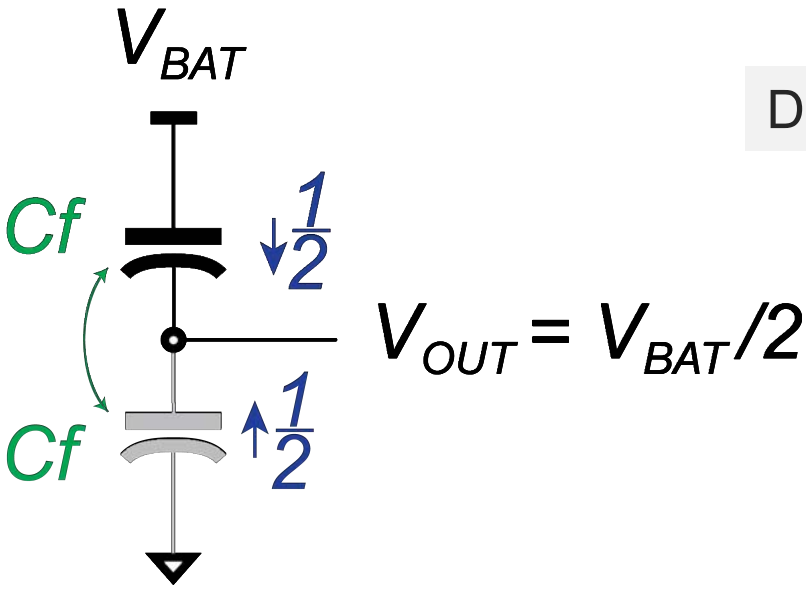
Goal of this work:
Realize a high density converter with high η

Outline

- New Class of DC-DC converters: Flying Power Domain
- Power Domain Interfacing Level Shifters
- All Digital Bang-Bang Control
- Measurement Results
- Summary

2:1 Switched Capacitor Topology

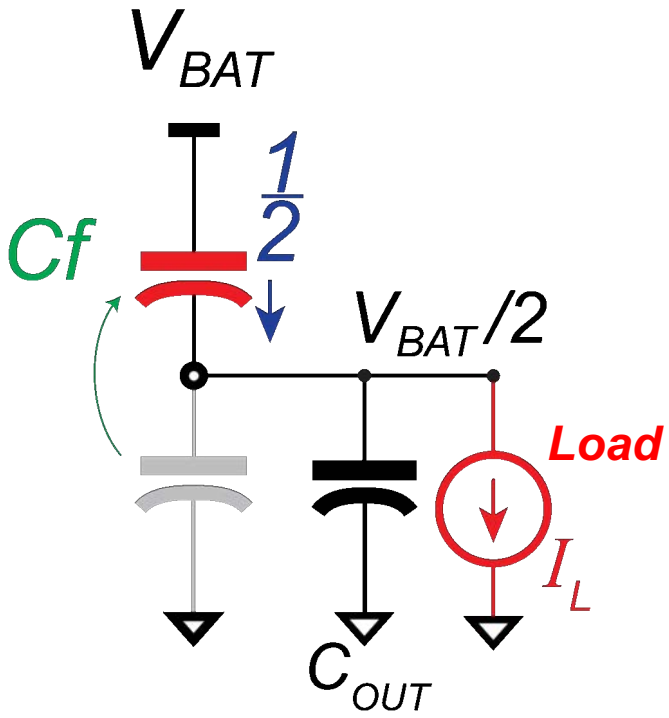


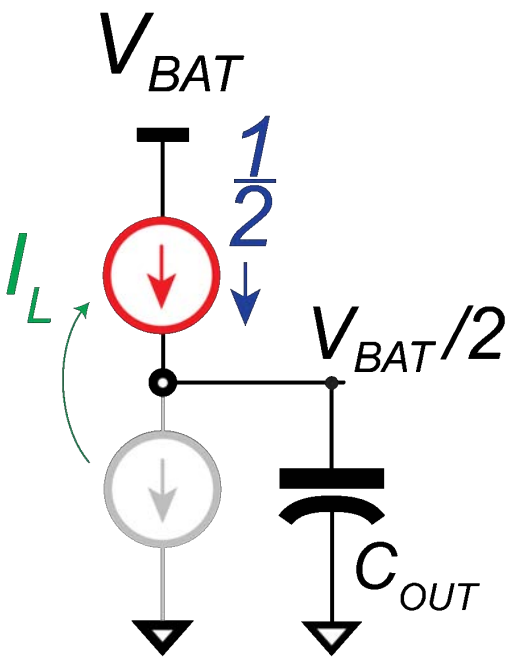


High-Density DC-DC via Circuit Techniques

- How to get rid of the area-consuming cap *Cf* ?

Switch the load itself instead of the cap





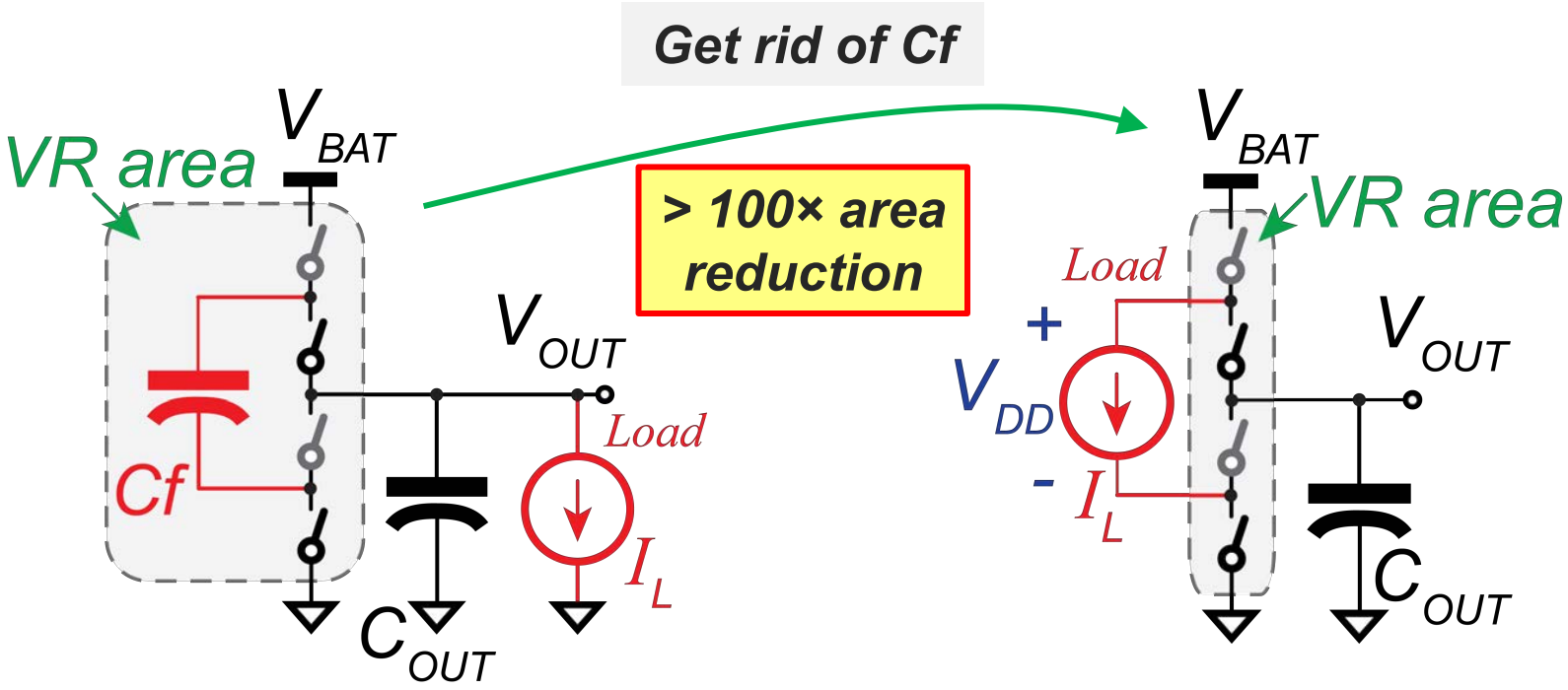
Cf **consumes > 99% of the converter area**

2-phase switched network KVL equations enforces $V_{LOAD} = V_{BAT}/2$

2:1 Flying Domain DC-DC Converter

- How to implement?
  - *Use 4 power switches to fly the load itself*

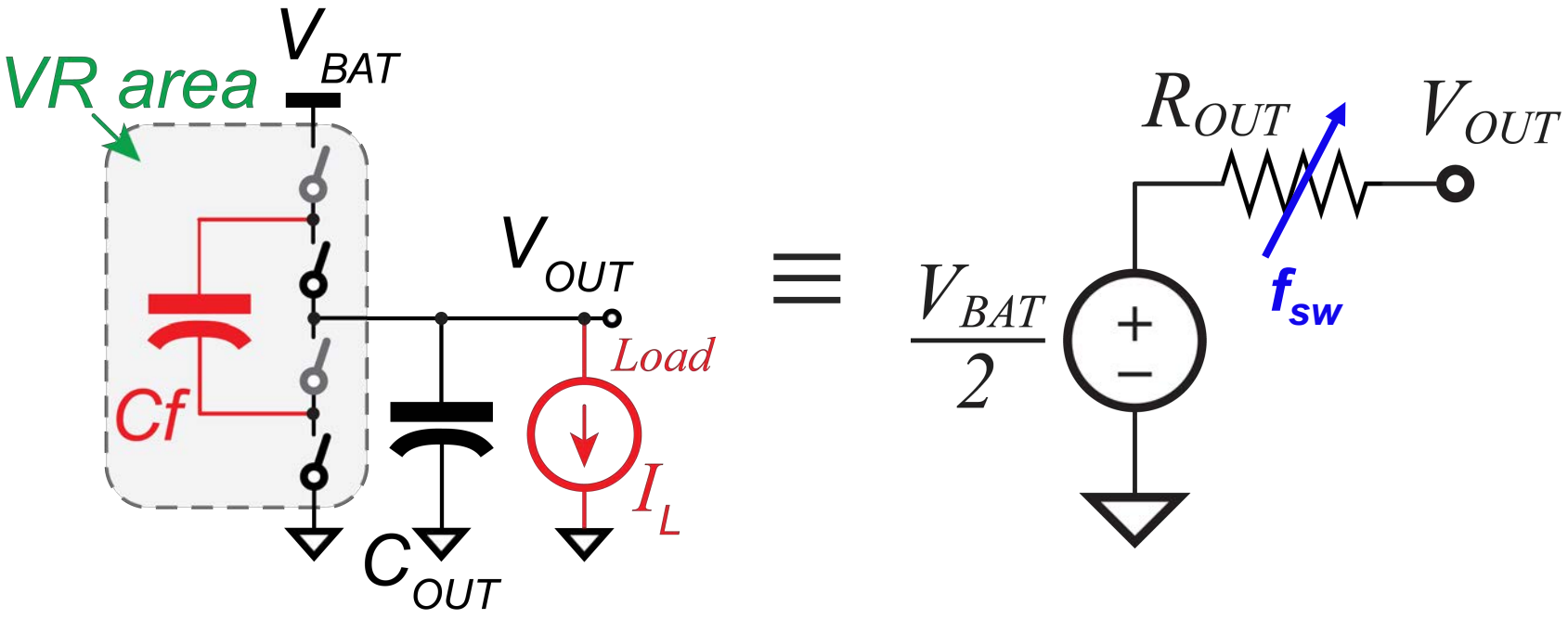
Switched Capacitor | **Switched Load (Flying Domain)**



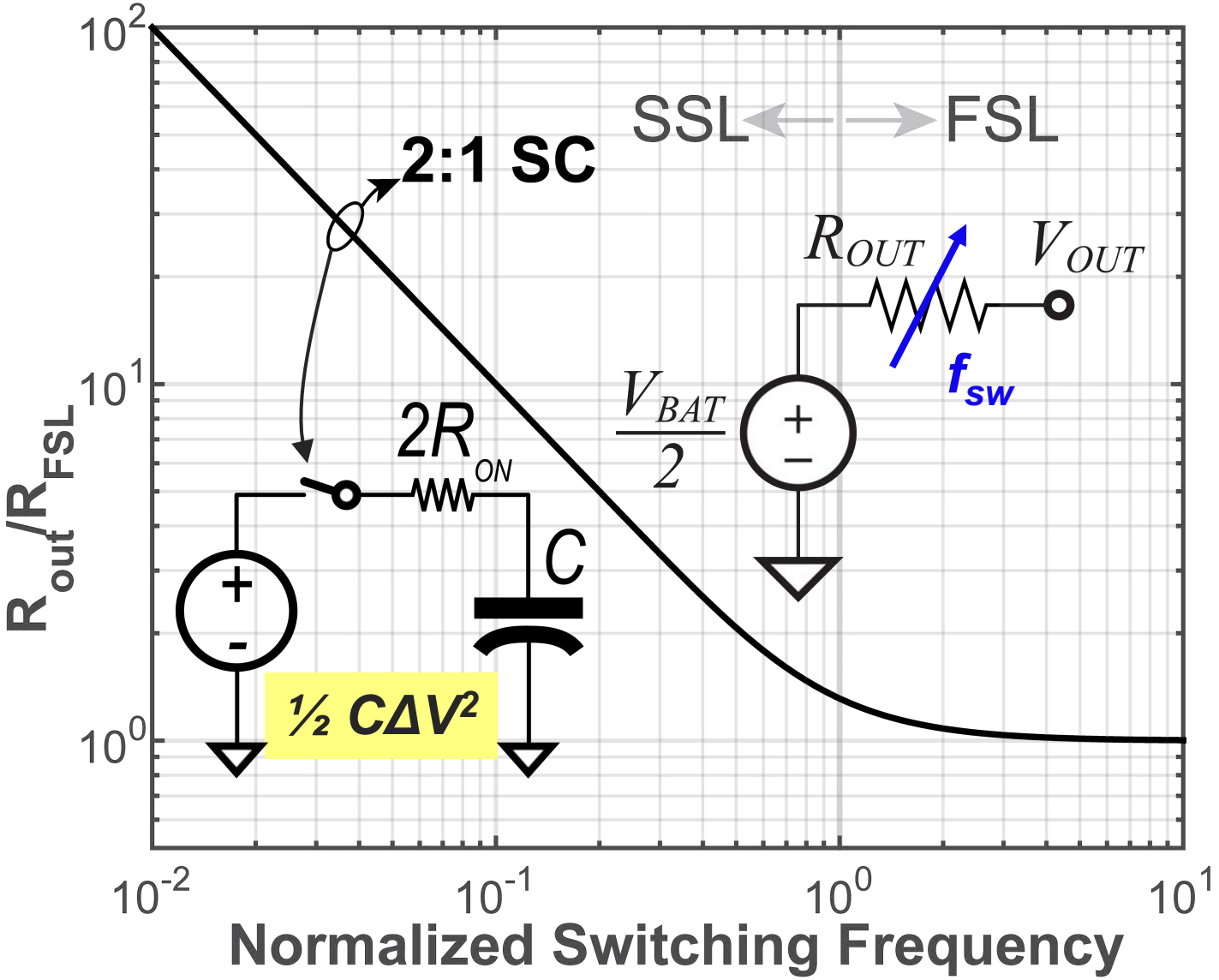
Switched Capacitor Loss Model

- Thevenin equivalent model

2:1 Switched Capacitor



Charge-Sharing Loss Elimination



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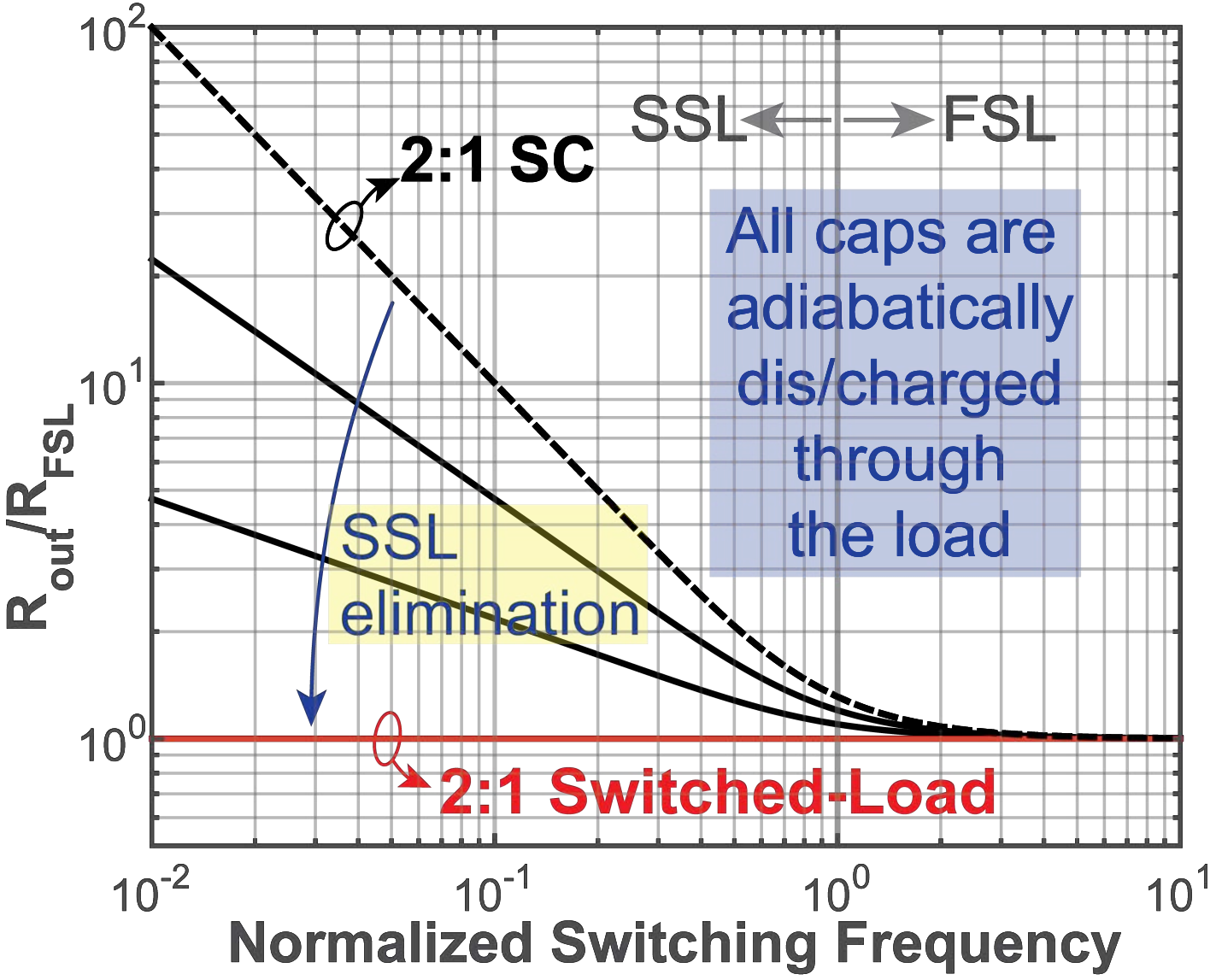
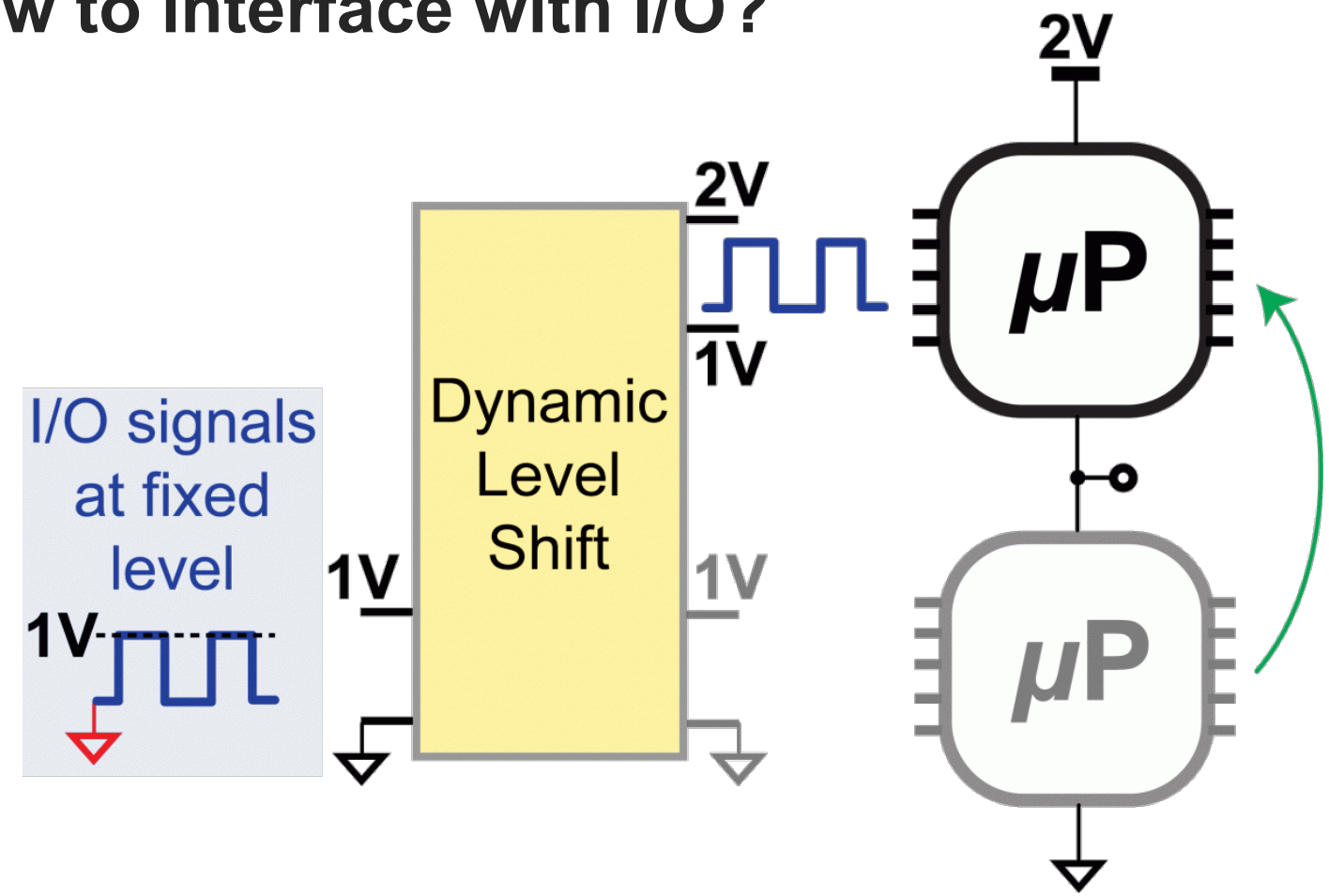


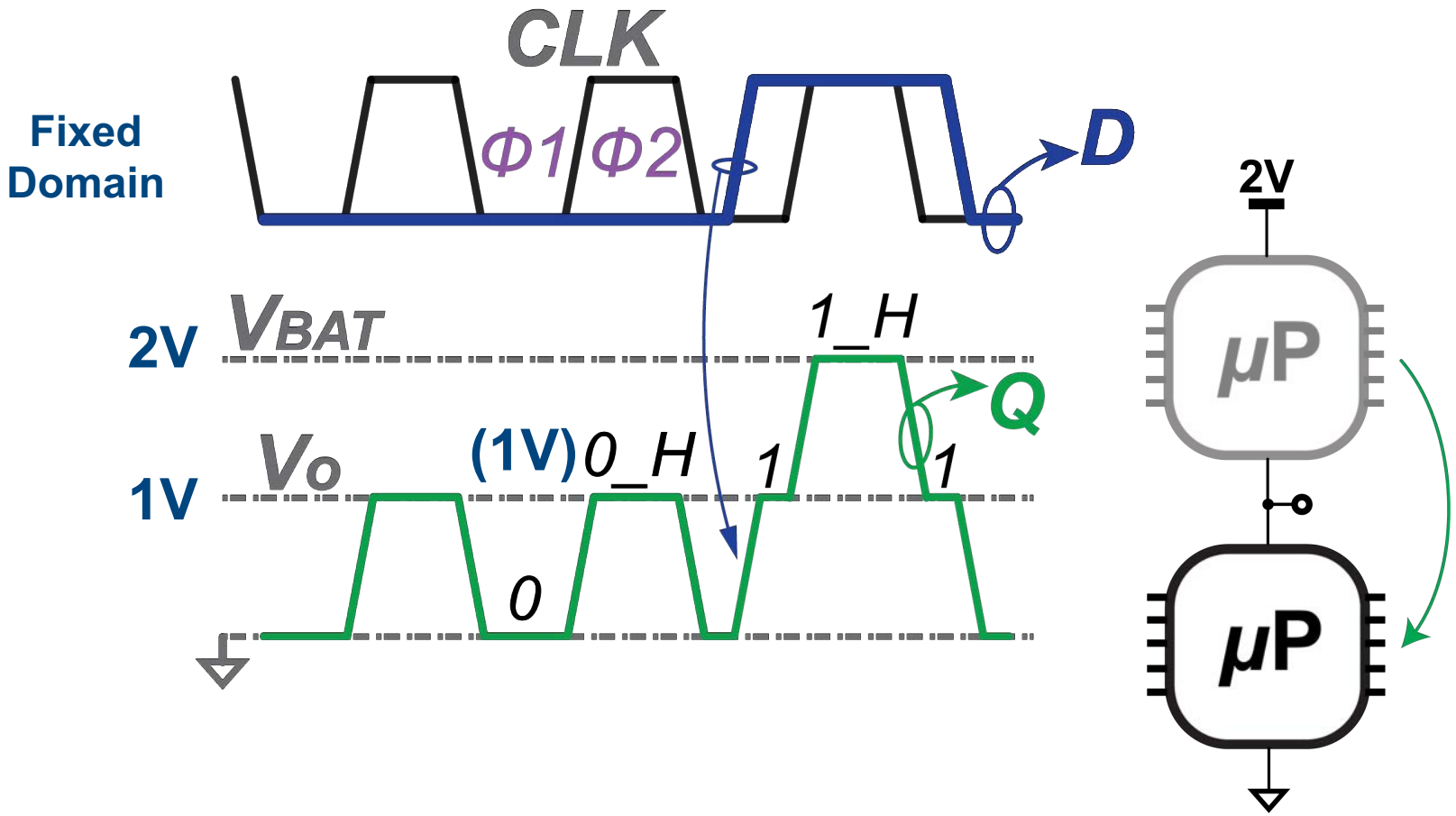
Level Shifting

- How to interface with I/O?



Inputs: require fixed-domain to flying-domain shifting
Outputs: require flying-domain to fixed-domain shifting

Sampling Level-Shifters

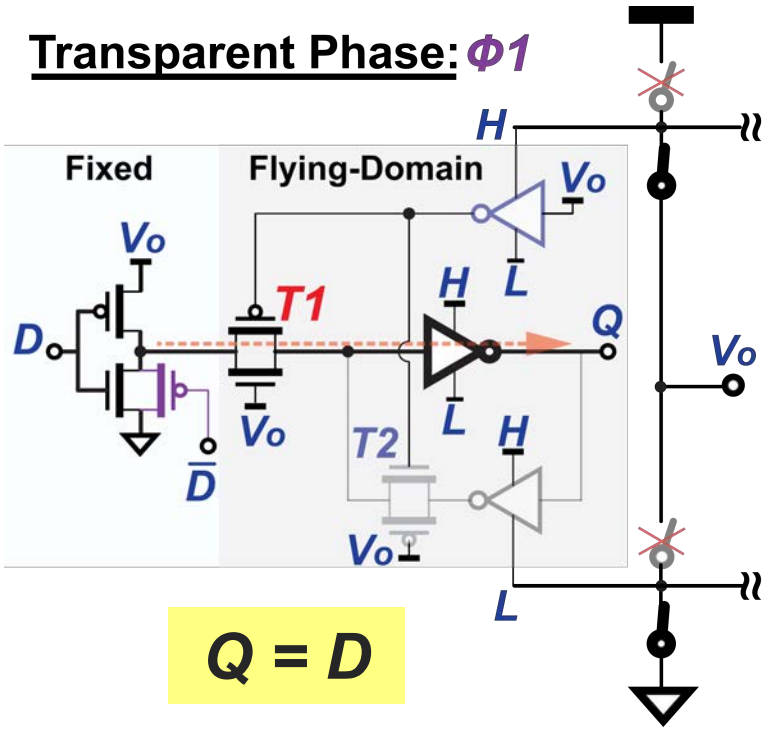


Requires
$f_{sampling} > 2f_{signal}$

A continuous shifter is available for faster signals; see paper

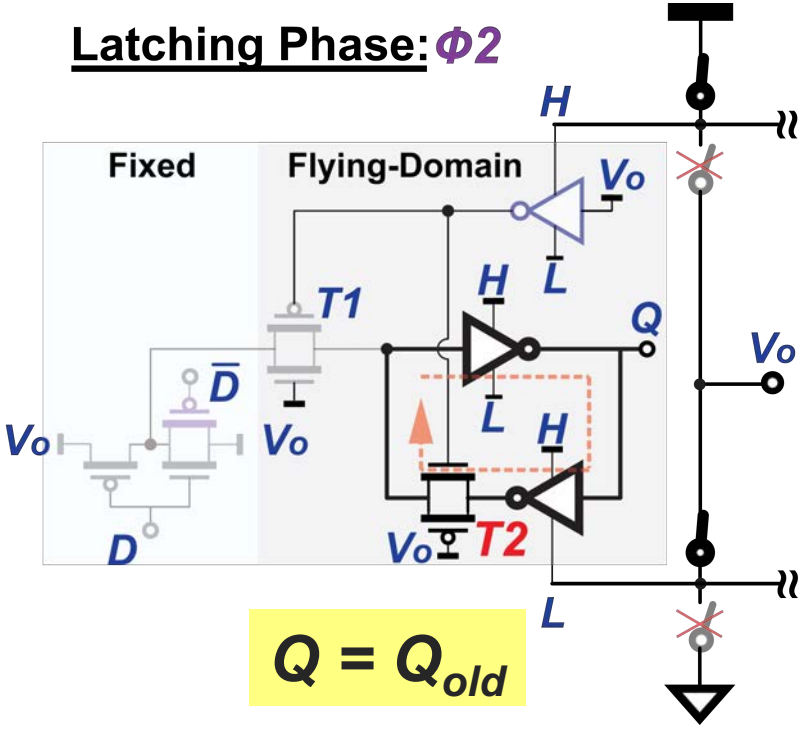
Sampling Level-Shifters

Transparent Phase: $\Phi 1$



$Q = D$

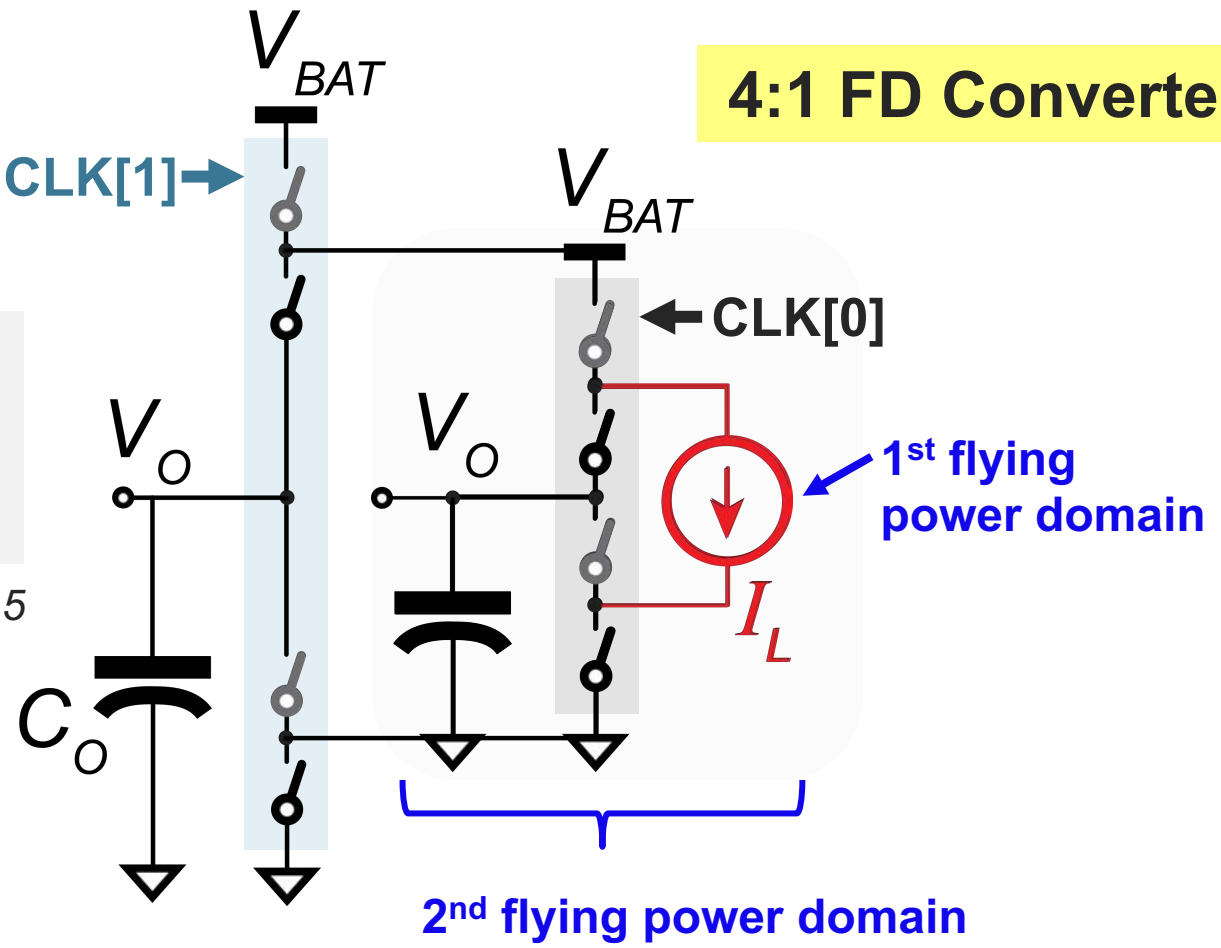
Latching Phase: $\Phi 2$



$Q = Q_{old}$

Multi-Ratio Flying Domain DC-DC Converter

- Fly the input terminals of the 2:1 cell through the switches of a 2nd FD converter: *4:1 FD converter*



$f_{CLK[1]} = f_{CLK[0]}/2$ for valid steady state

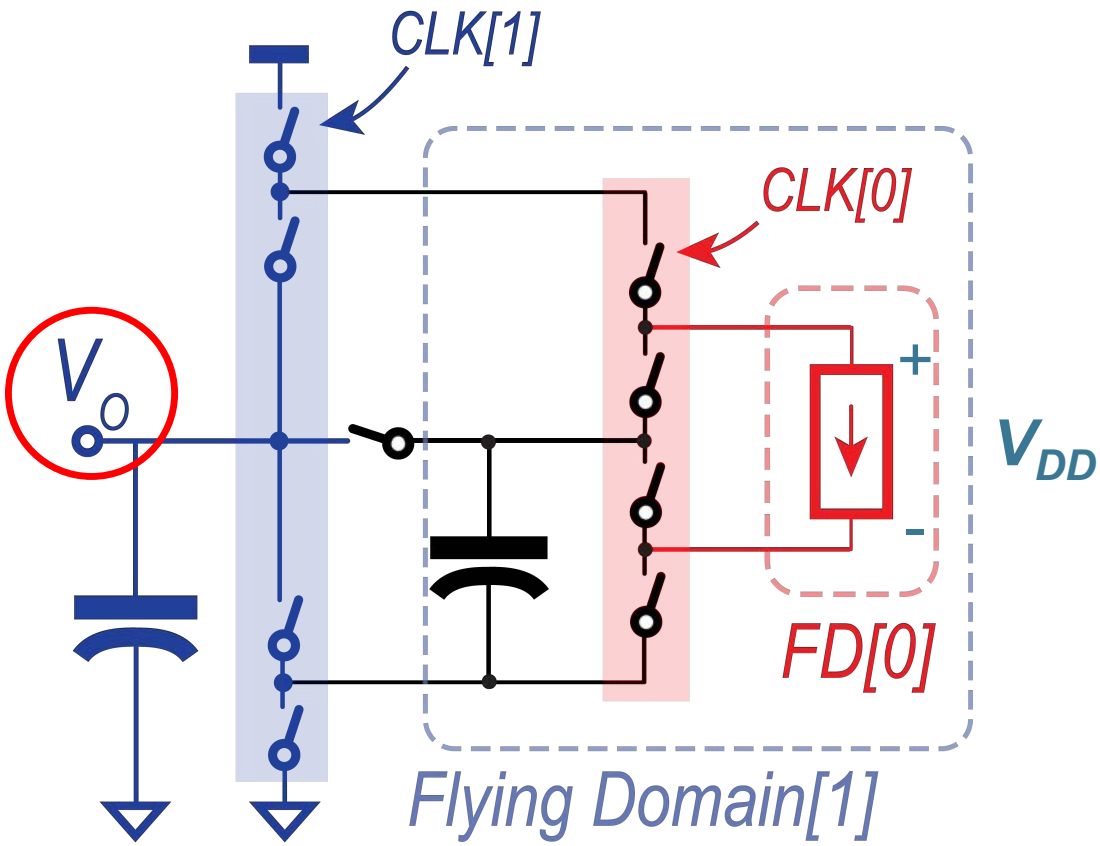
†Salem & Mercier, VLSI'15

Bang-Bang Control

- Load voltage is observable through V_o

Observable in both ratio settings

Easy to perform Freq. Modulation



Bang-Bang Control

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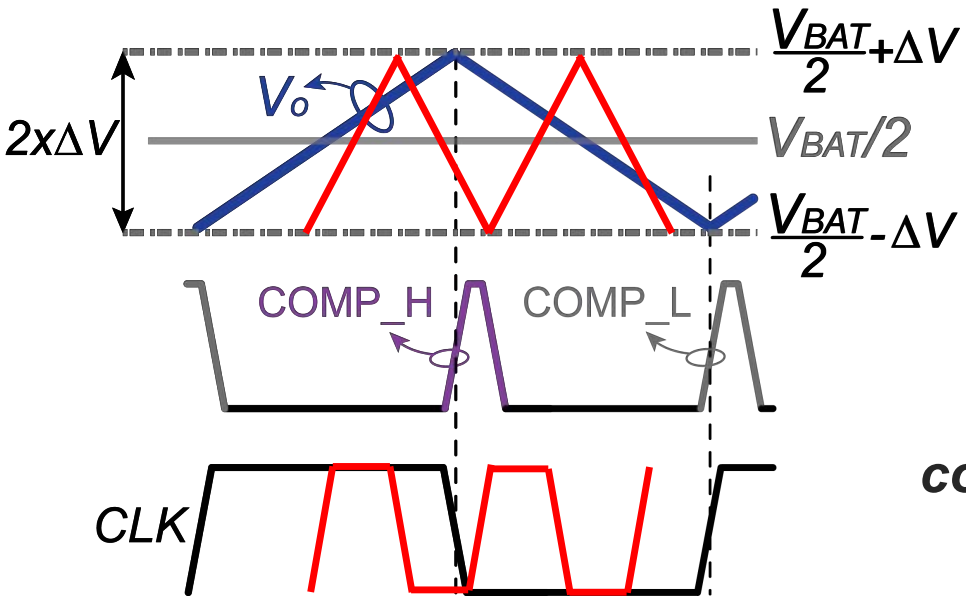
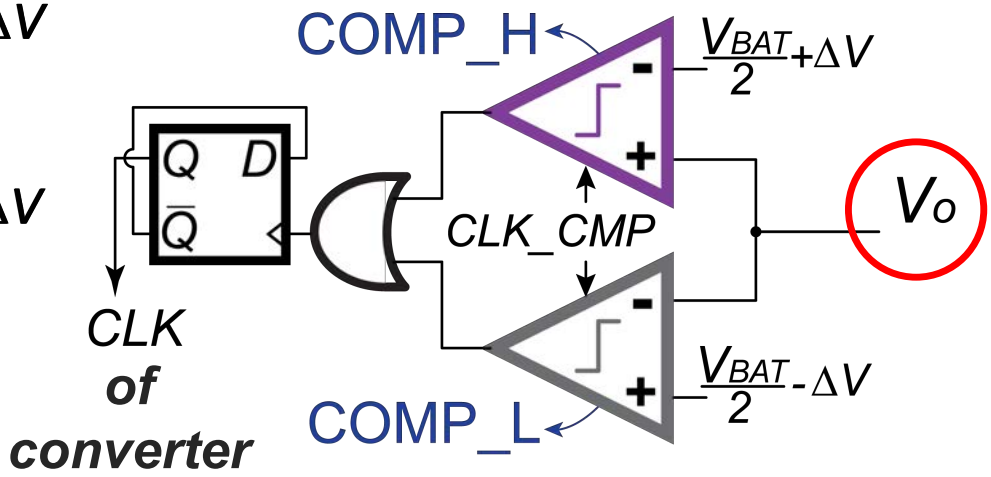
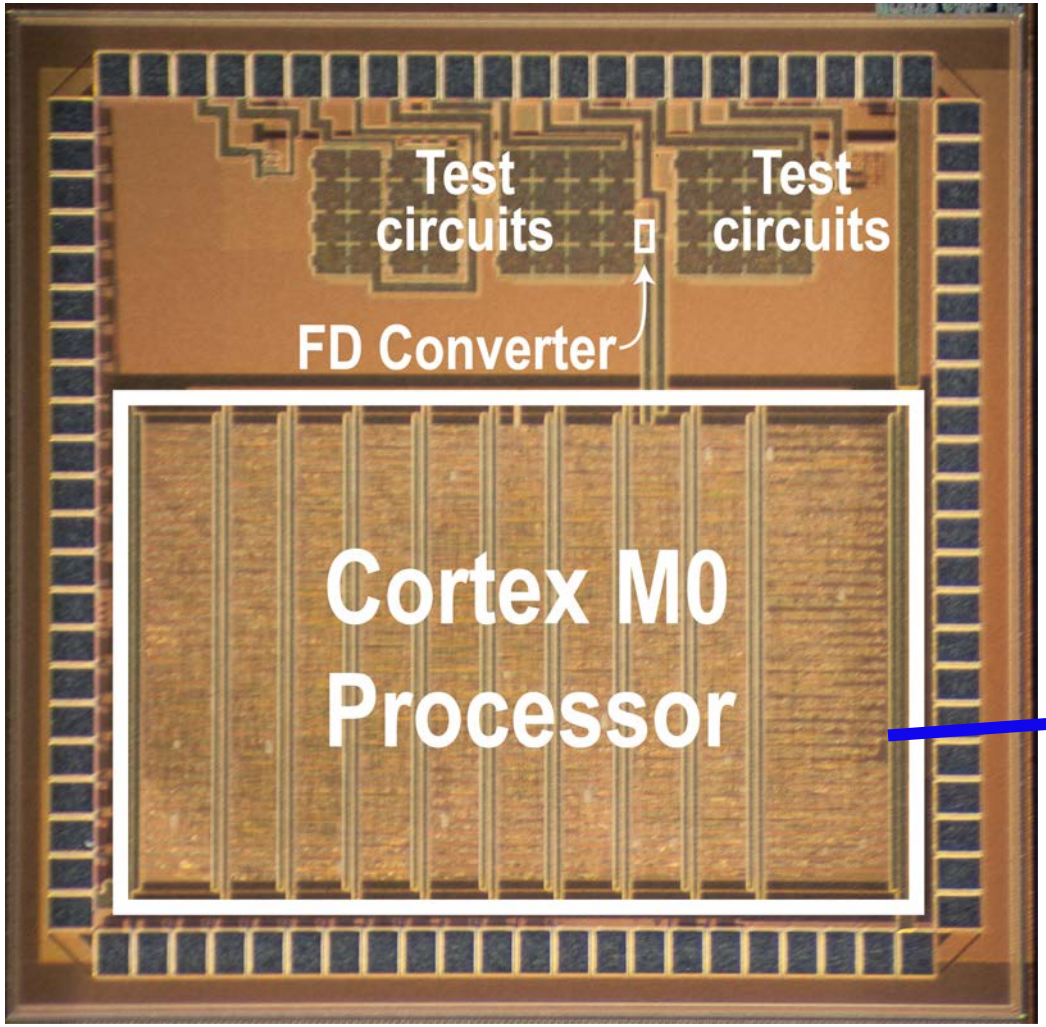




All-digital Bang-Bang Controller

Scales switching parasitics with load current for high light-load η

Flying Domain Converter Prototype

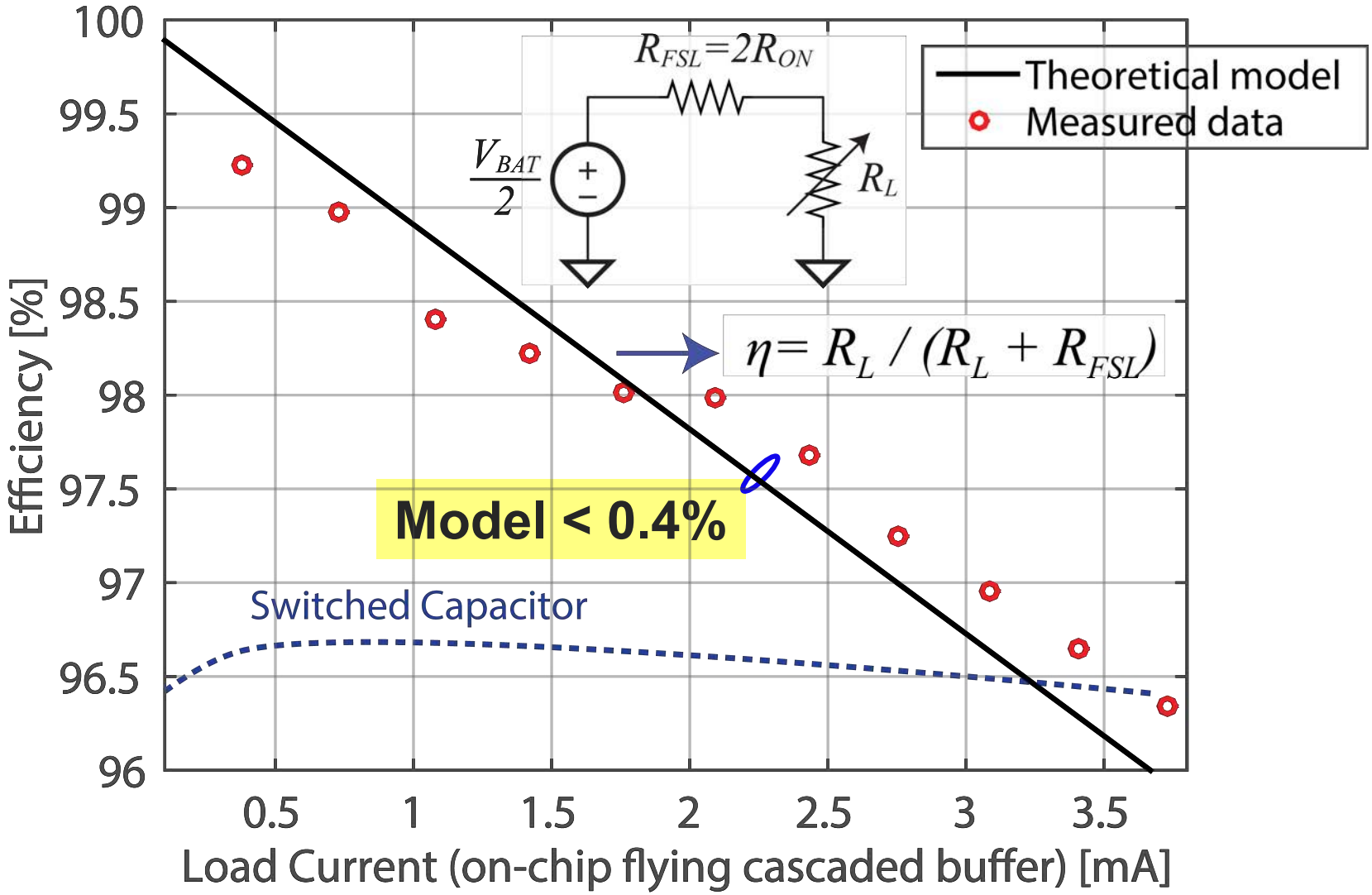


Tech.	*0.18μm SOI*
V_{IN}	*0.4 - 3V*

1.95mm²

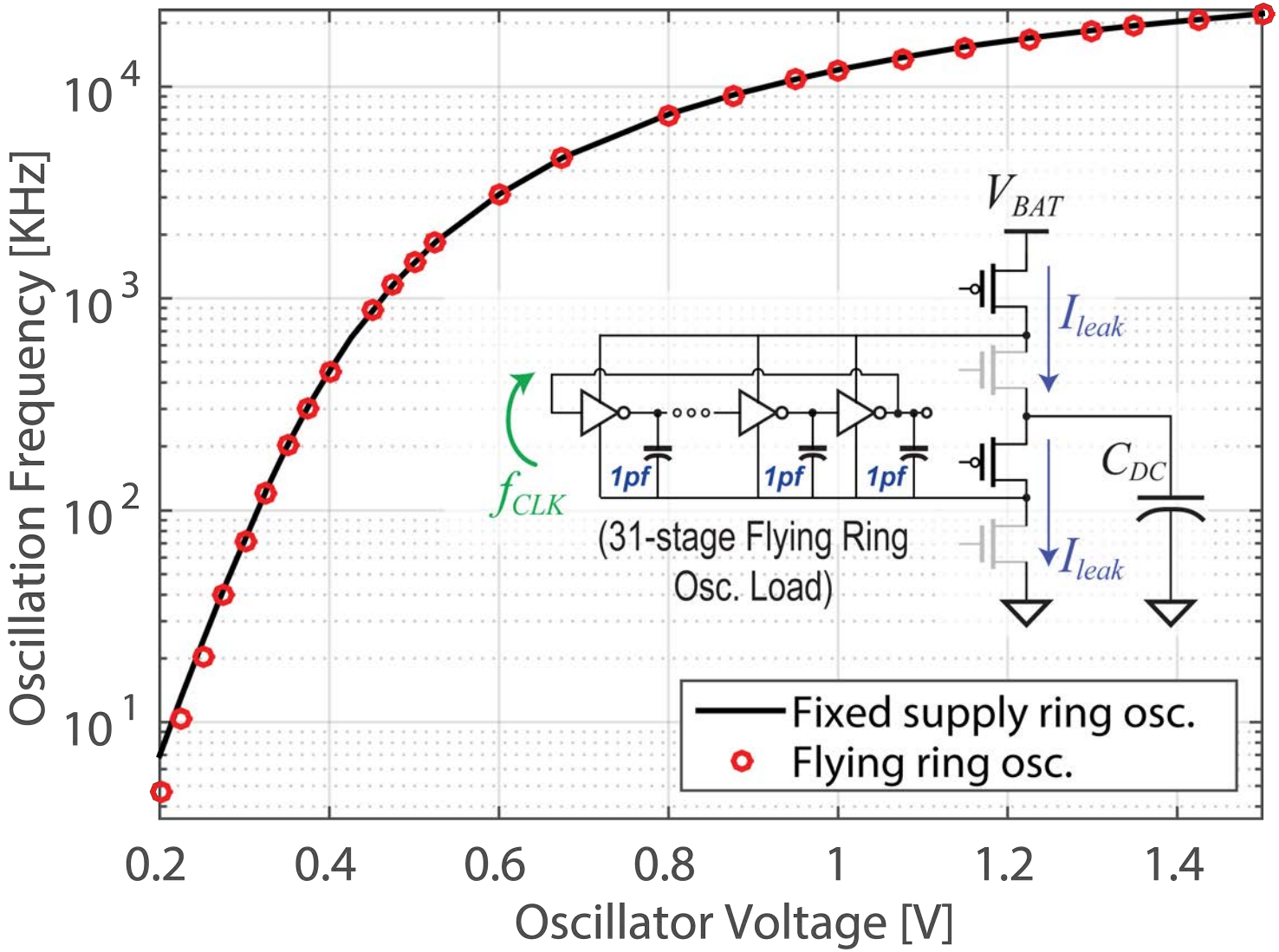
Measured Efficiency vs. I_L

η increases at light loads (no charge-sharing loss)



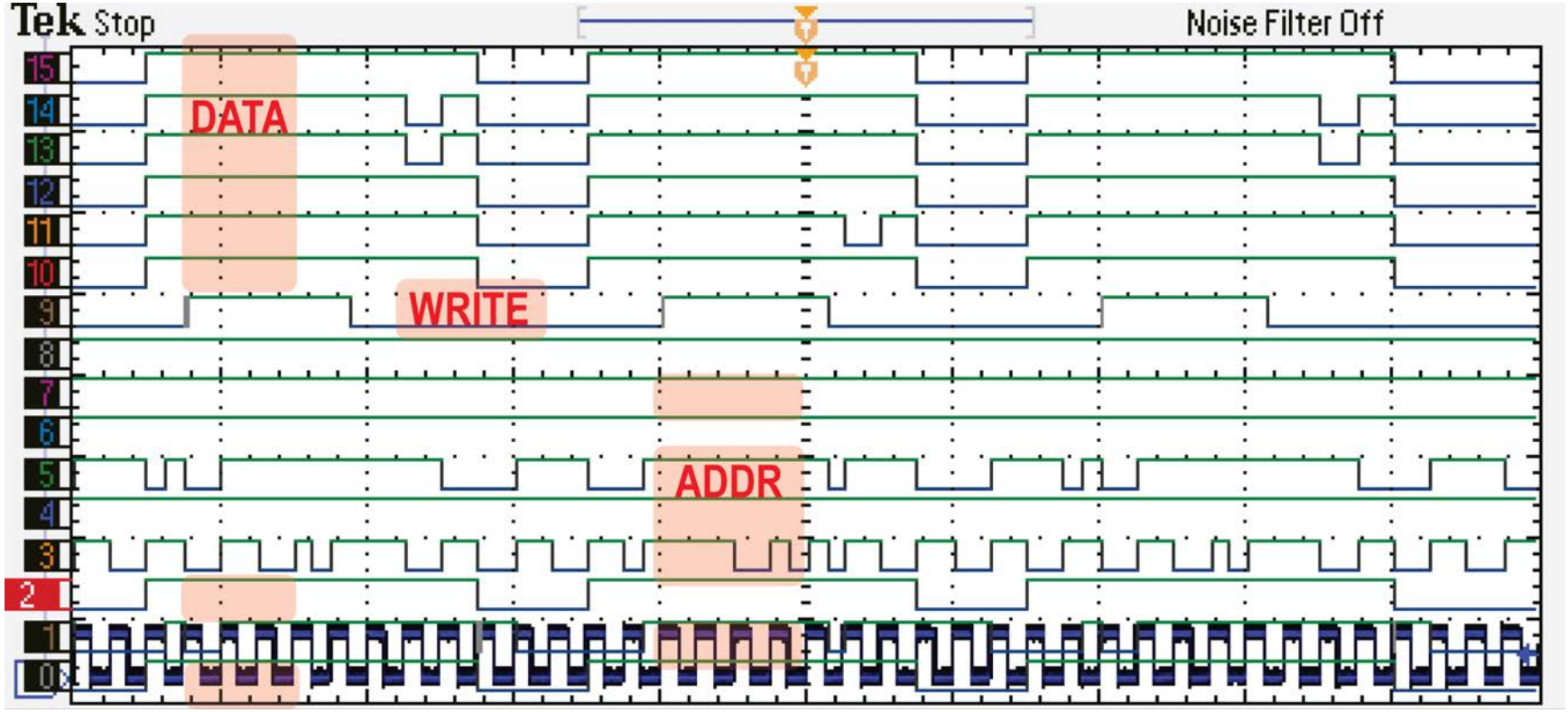
Measured Ring Osc. Frequency

Freq. error < 2% for V_{OSC} = 0.4-to-1.5V at η = 96%



Measured ARM Cortex Output Waveforms

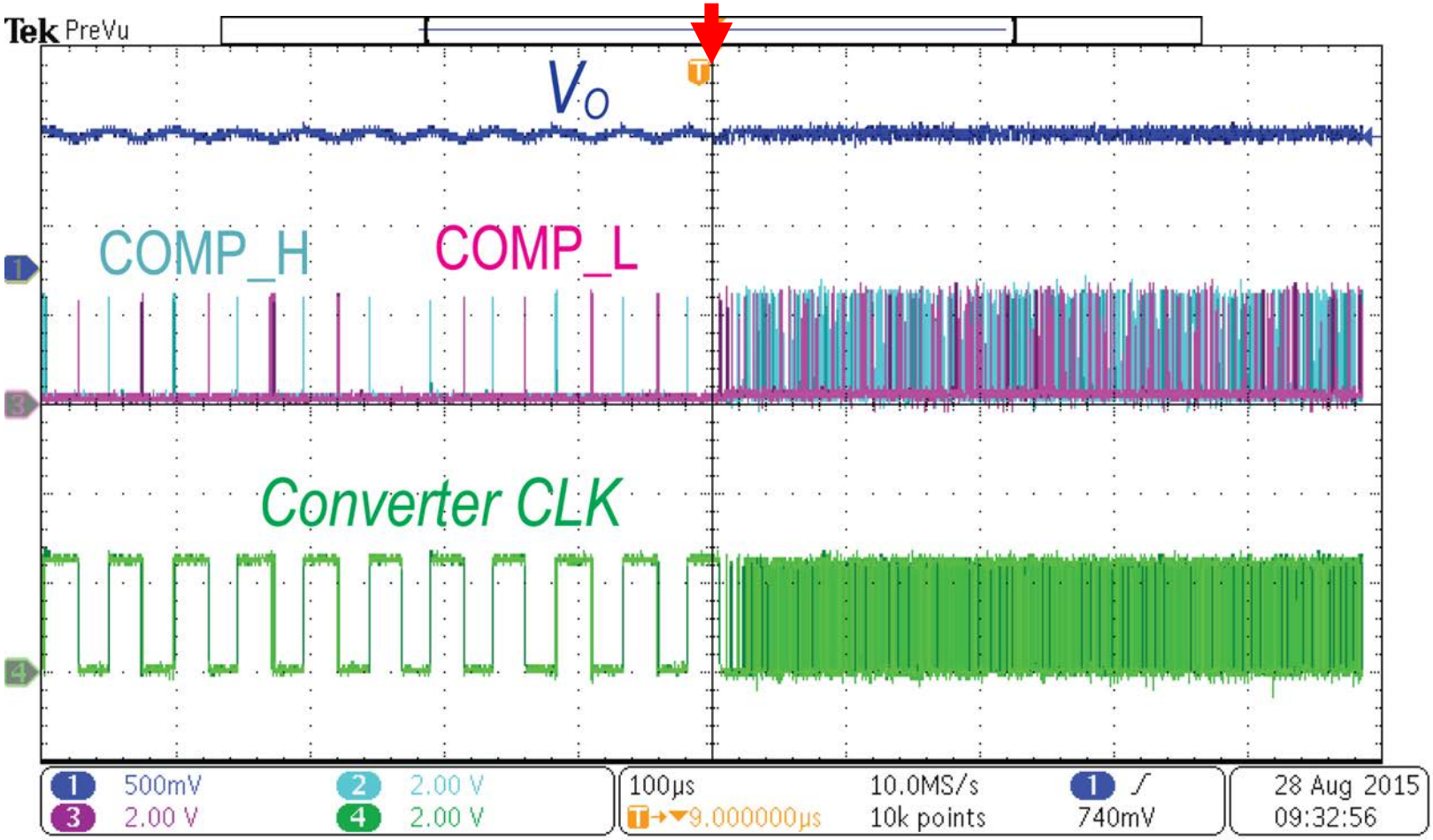
Flying the entire 1.95mm² µP: η = 90.8% at ($I_{\mu P}$=3.63mA, V_{BAT}=3V), while running a checksum program at 1MHz



Outputs after flying to fixed shifters

Measured Controller Waveforms

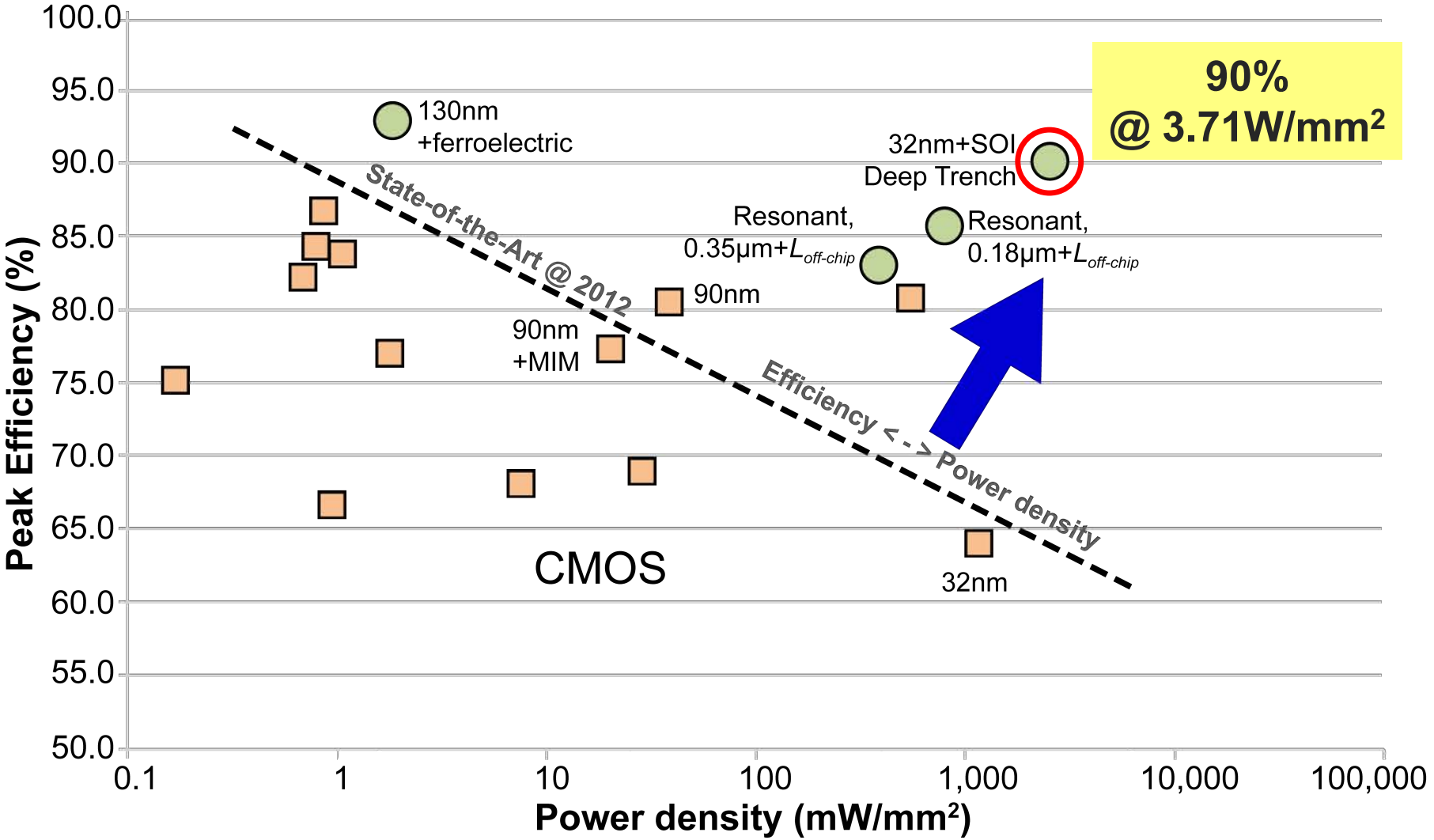
Sudden I_L step: 21.8μA→1mA



response time ~ 330ns, 50mV$_{p\text{-}p}$

State of The Art

- Peak efficiency vs. power density



* Plot based on 2015 ISSCC Trends press document

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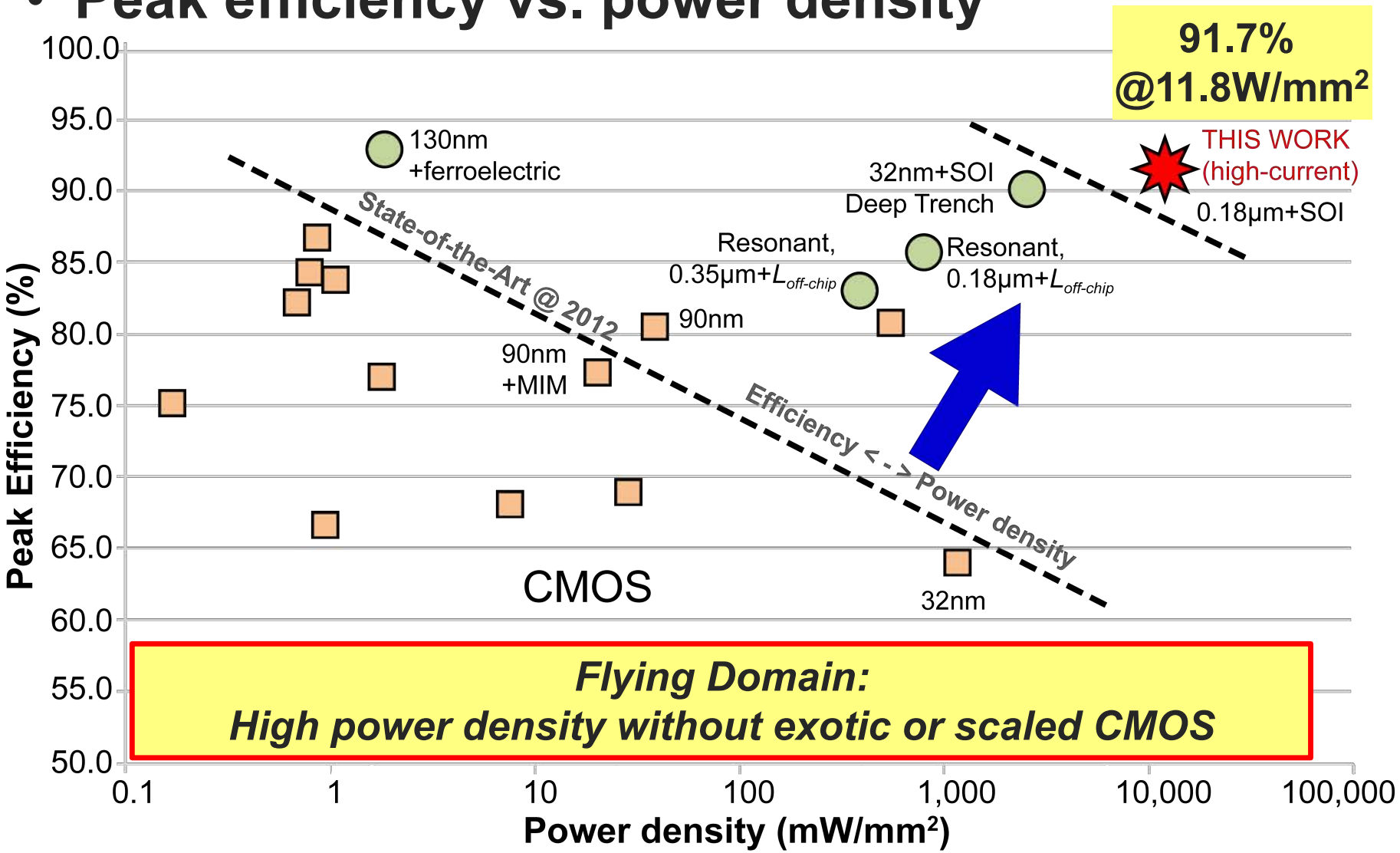

* Plot based on 2015 ISSCC Trends press document

Summary

- *A new class of DC-DC converters, flying-domain*
  - Load is directly switched, instead of a passive, in a 2:1 topology, increasing power density
  - Requires SOI & doesn't eliminate C_{out}

SSL elimination

Cf elimination

High η @ high Power density