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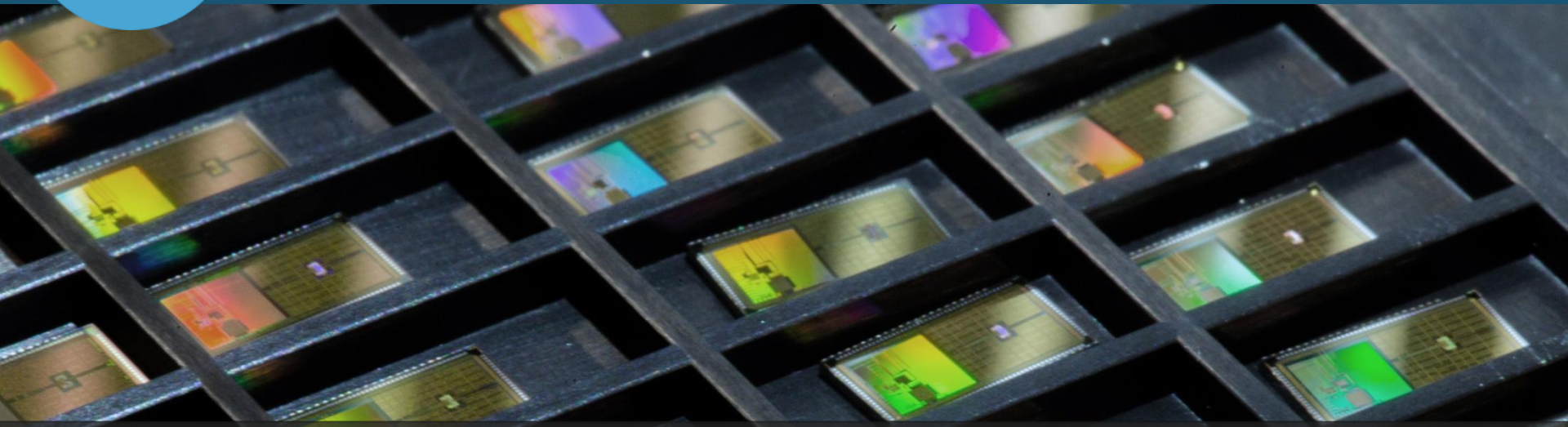
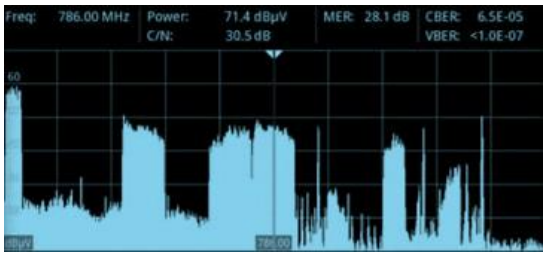


A Recursive House-of-Cards Digital Power Amplifier Employing a λ/4-less Doherty Power Combiner in 65nm CMOS

Loai G. Salem, James F. Buckwalter, and Patrick P. Mercier

University of California, San Diego

Motivation: PA design in 5G and Beyond



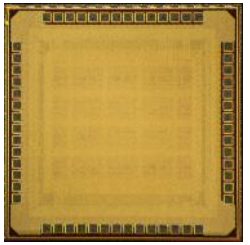
5G Need
Circuit Requirement

Spectral Efficiency
Linearity

Battery life
Efficiency

Cost
CMOS integration

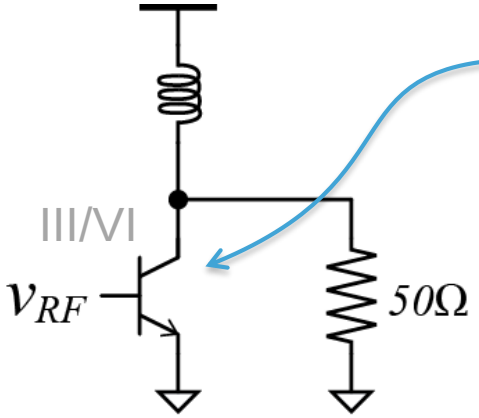
Communication range
High output power



Conventional PA Design

It is difficult for PAs to *simultaneously* achieve high output power, efficiency, and linearity in scaled CMOS

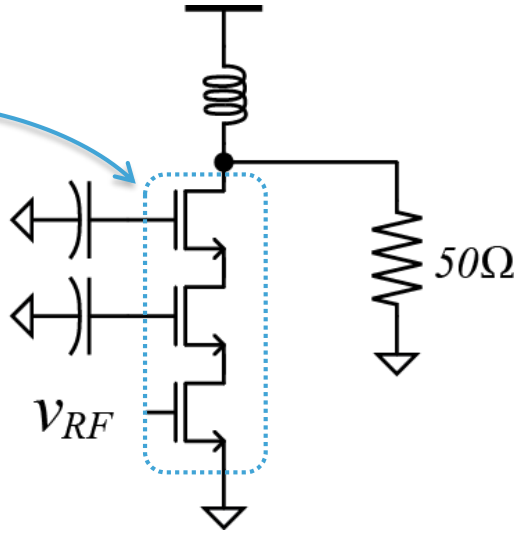
Conventional PA design:



PROS: high output power, good linearity
CONS: not CMOS integrated, poor efficiency

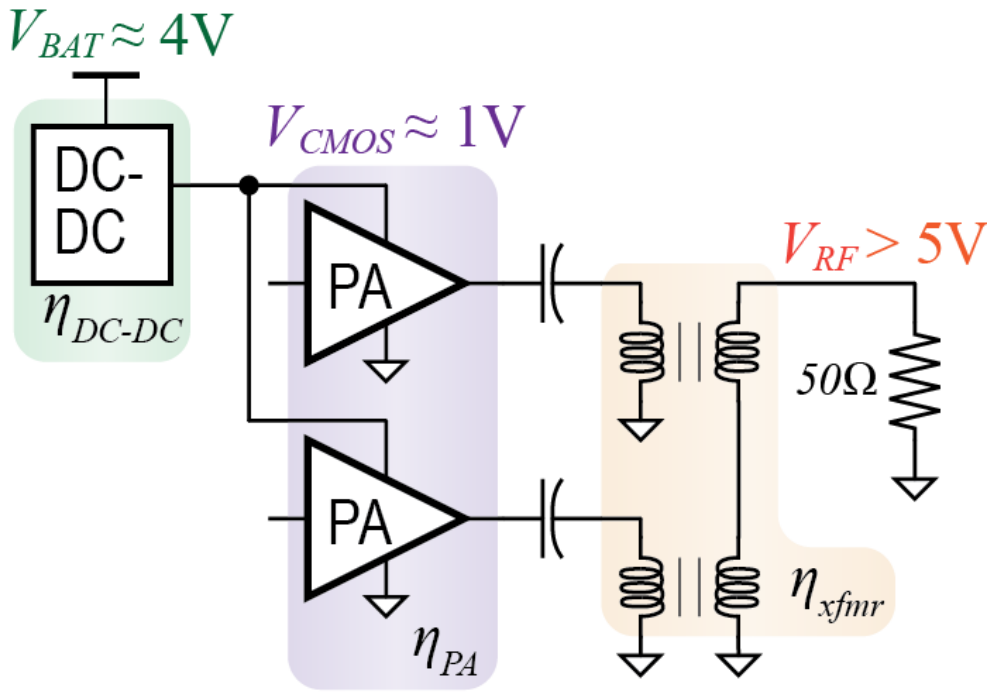
Linear transconductor

Transistor stacking:



PROS: CMOS integration
CONS: poor efficiency & linearity
→ **scaled CMOS transistors are not good transconductors!**

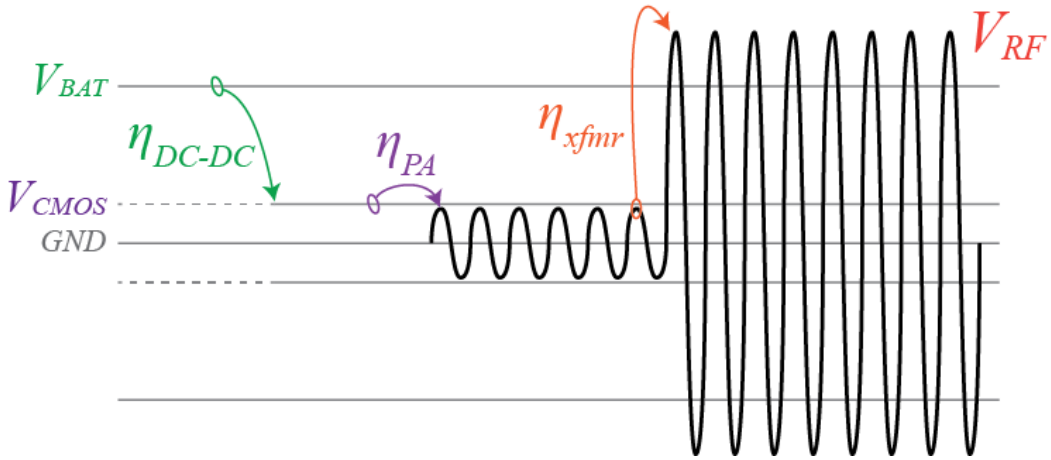
Prior work: CMOS Power Combining



Idea: utilize many efficient ~1V class-D PAs and combine power with transformers

Problem: three voltage conversion stages leads to cascaded losses:

$$\eta_{tot} = \eta_{DC-DC}\,\eta_{PA}\,\eta_{xfmr} < 30\%$$



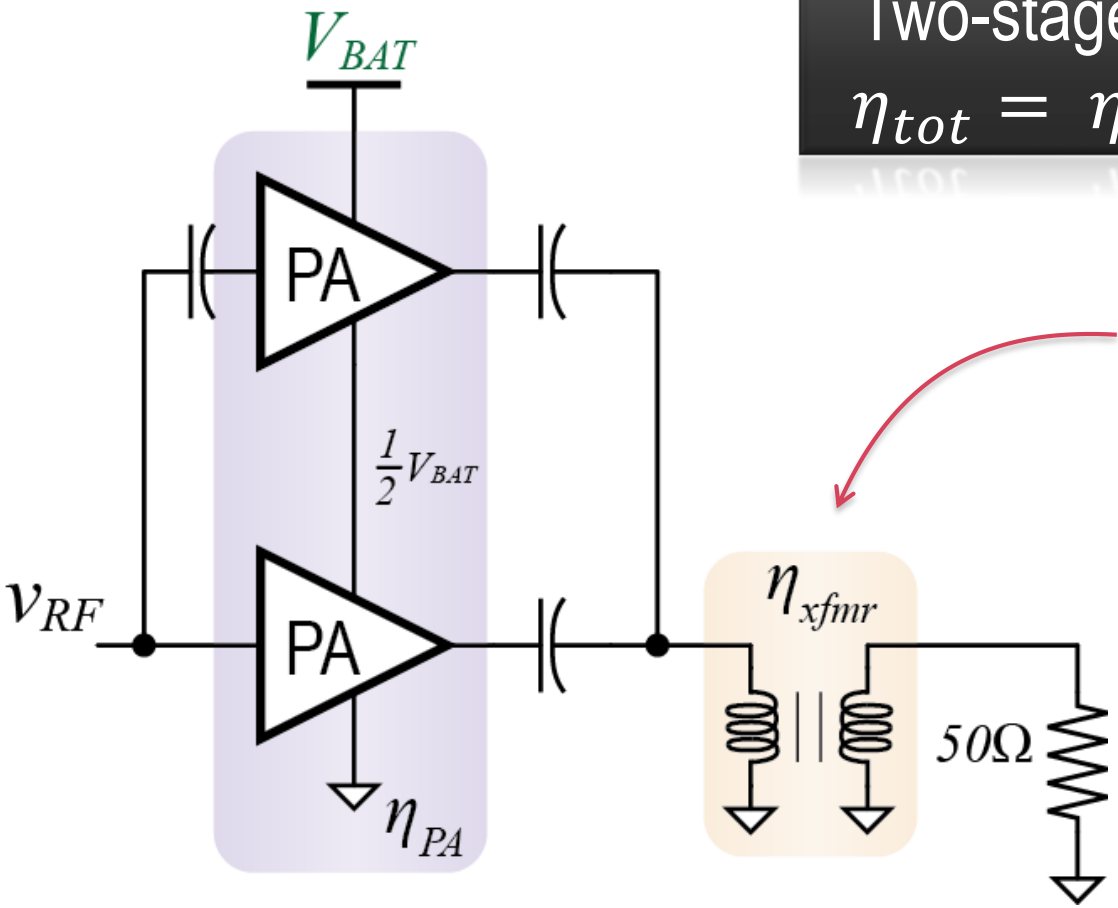
Why do we go down, then back up in voltage?
There must be a better way!

Partial Solution: PA Stacking

Stack entire class-D PAs for current re-use:

~100% efficient *implicit* DC-DC conversion

(each PA sees only $V_{BAT}/2$)



Two-stage cascade:

$$\eta_{tot} = \eta_{PA}\,\eta_{xfmr}$$

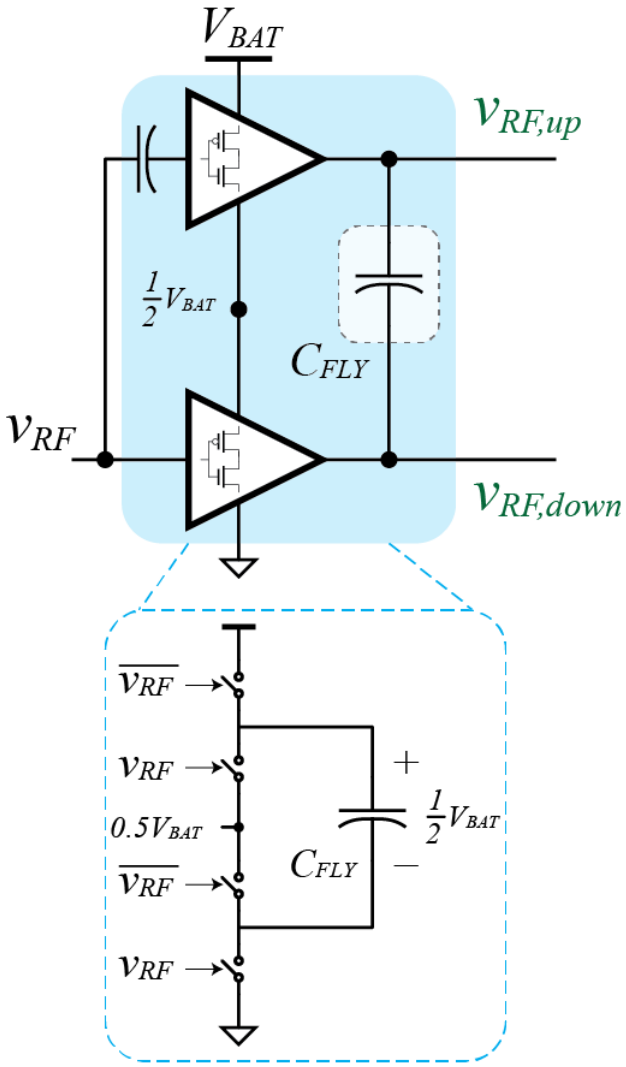
Problem 1: still require lossy transformer to achieve high output power in scaled CMOS

Problem 2: how to control P_{out} and mismatch charge?

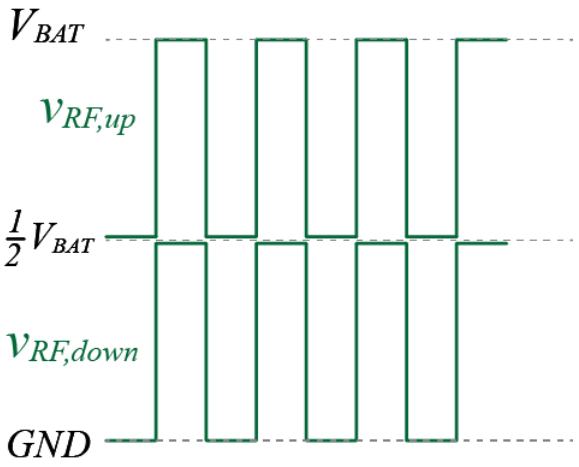
→ Discussed later

Solid-State RF Impedance Transformation

Idea: generate large RF voltages directly from a battery using ~1V devices by stacking PAs, then flying subsequent PAs between the rails of the prior stages in a *House-of-Cards* Topology



Animation not seen in print



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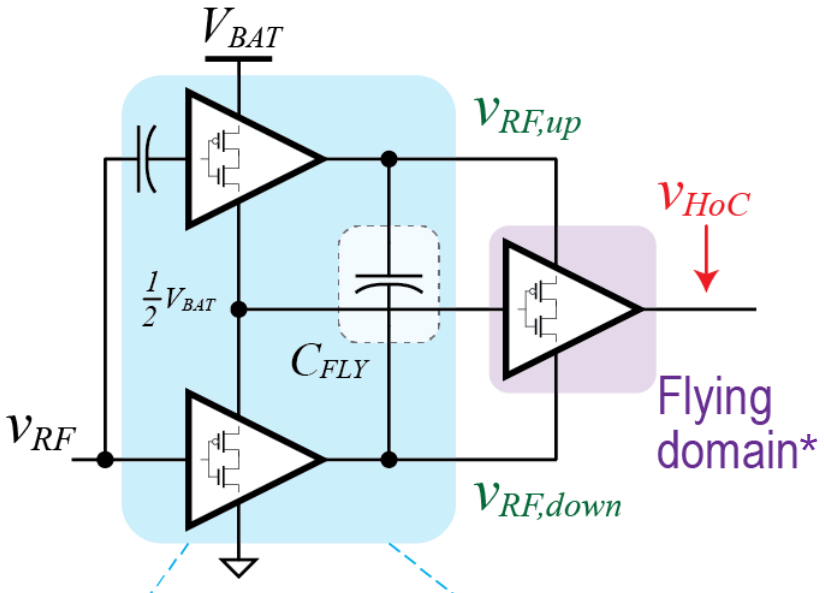

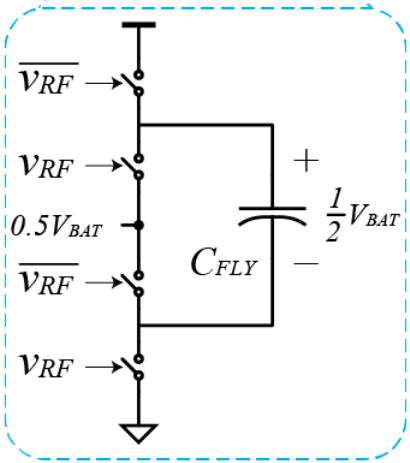

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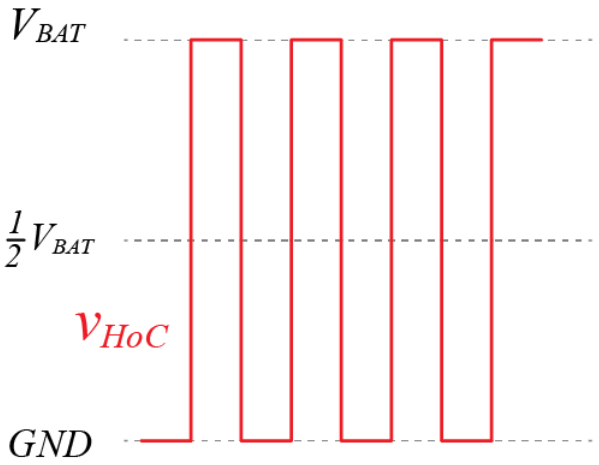

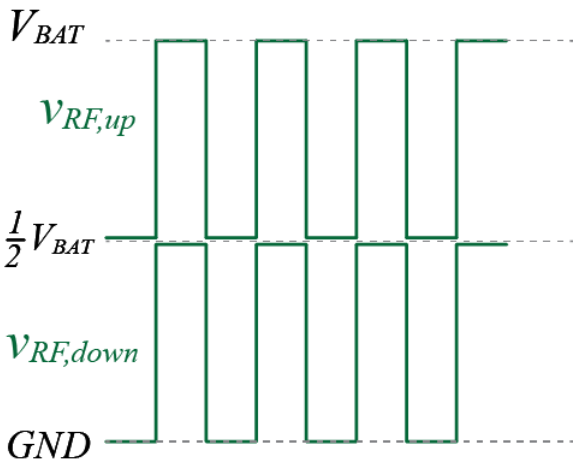

*For more information, see Salem et al., ISSCC'16

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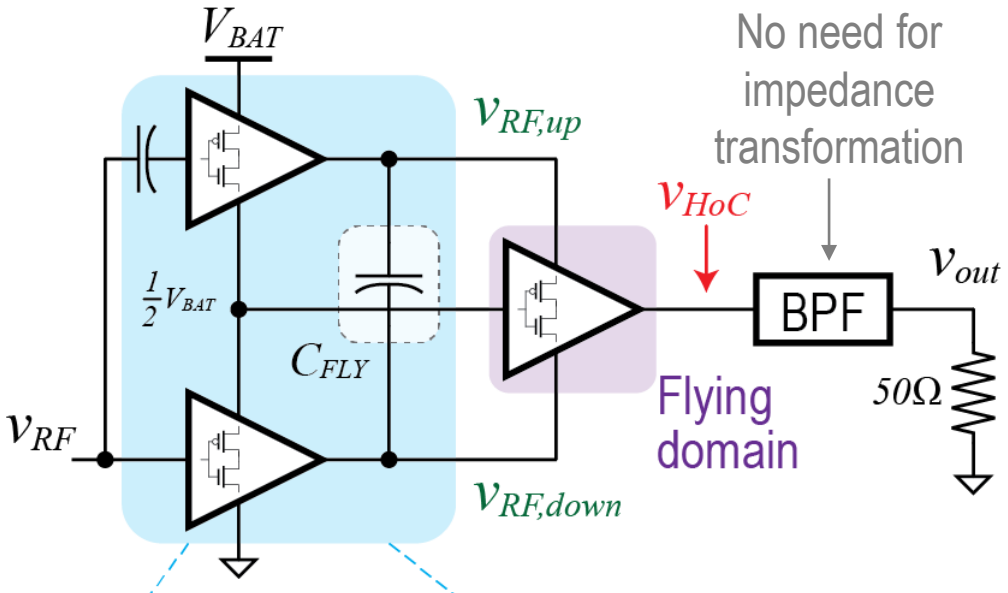
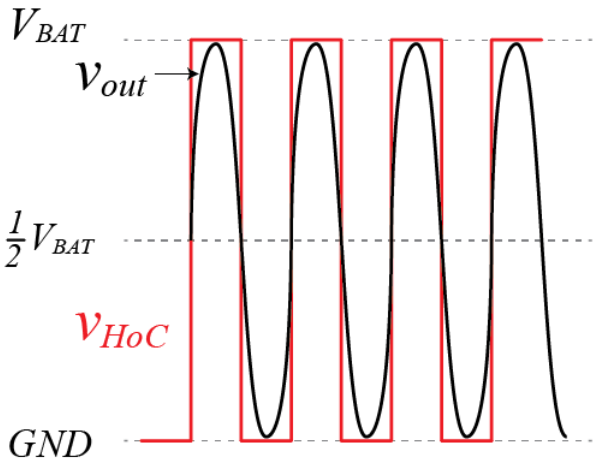
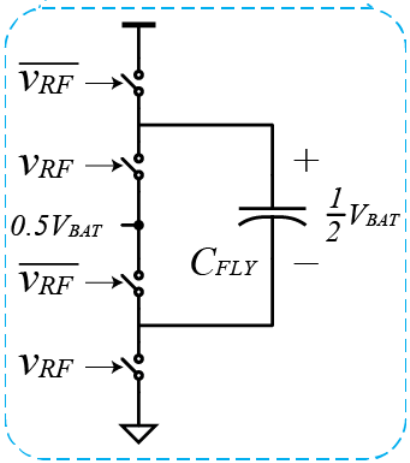
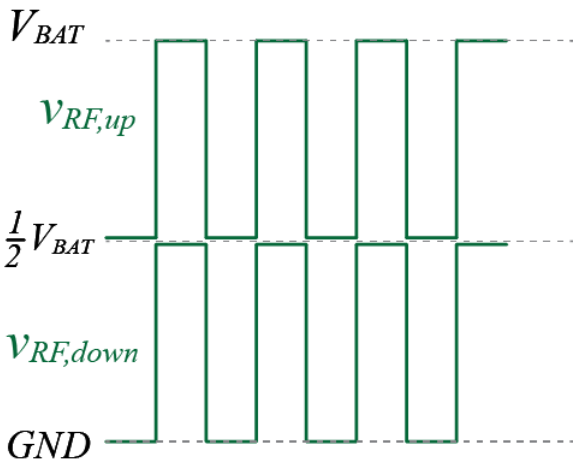






High power RF waveform synthesized directly from V_{BAT} using low-voltage transistors



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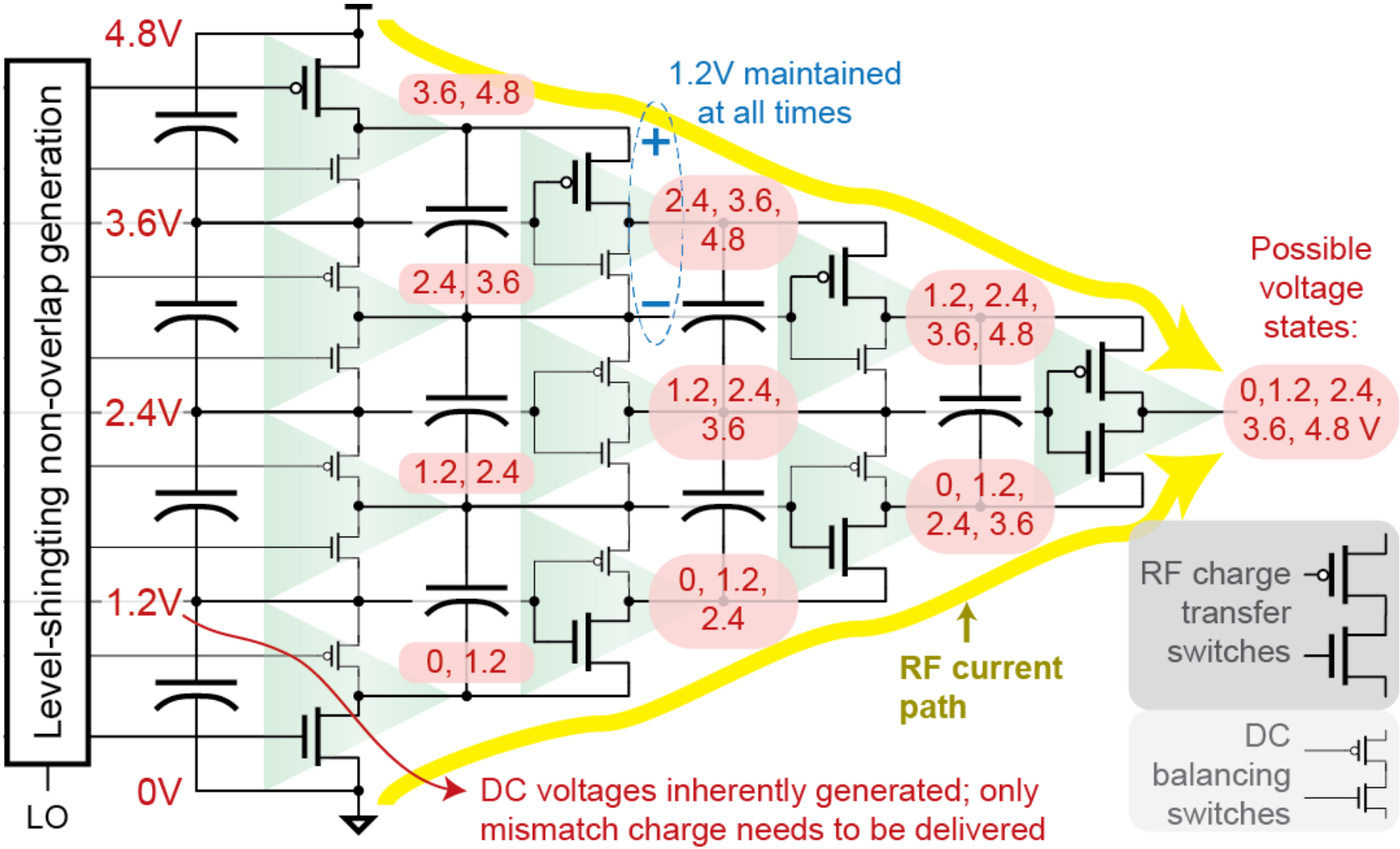
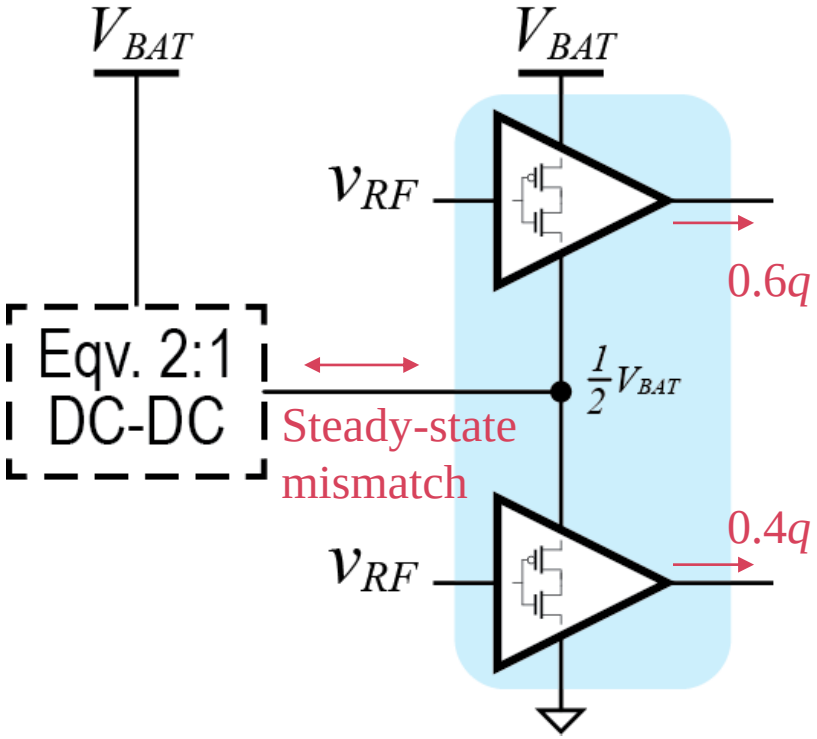
House-of-Cards (HoC) Schematic

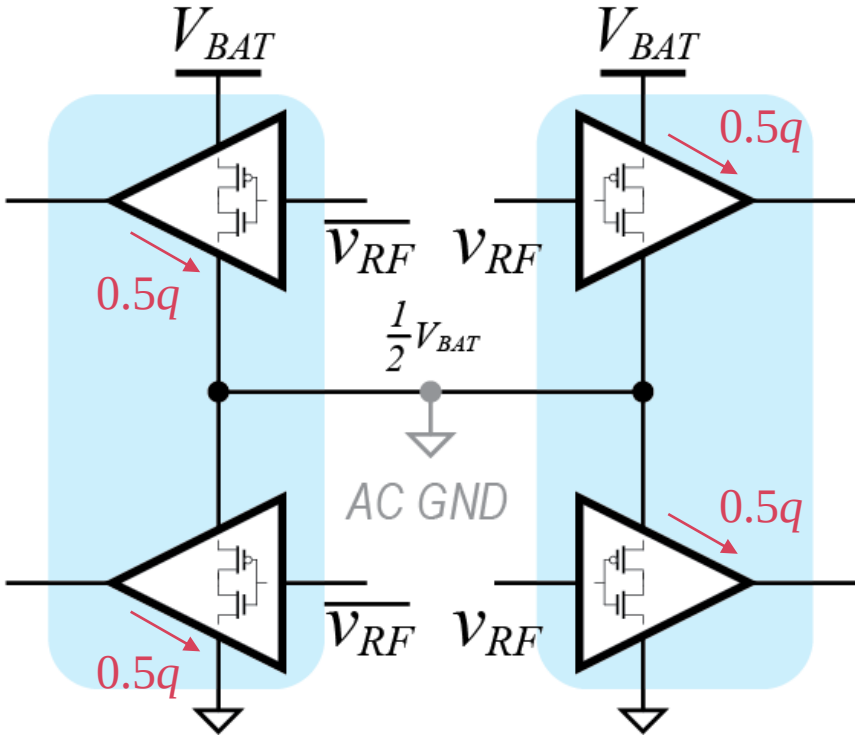


Managing Mismatch Charge

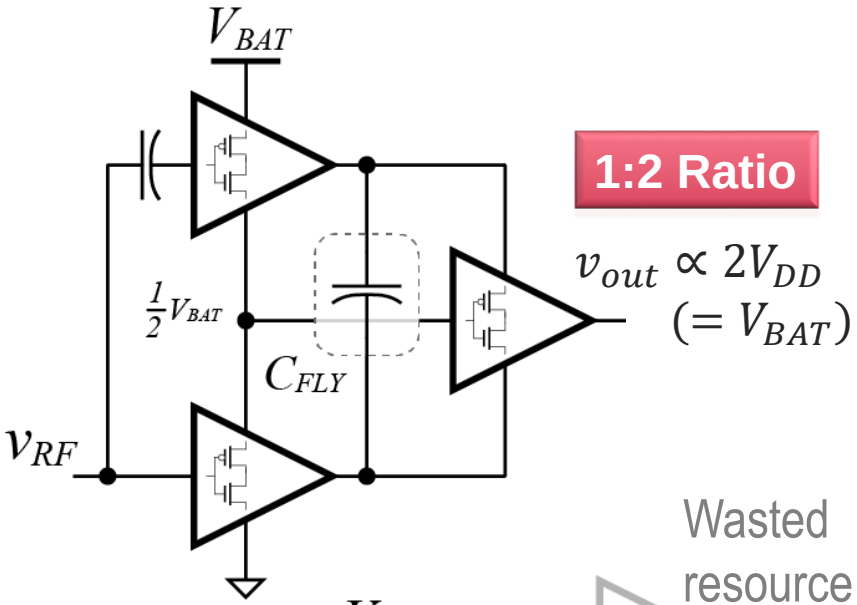
Problem: DC-DC converter nominally required to supply mismatch charge; adds cascaded losses

Solution: Differential architecture eliminates inter-domain loading and creates AC grounds; results in ~100% efficient DC-DC conversion





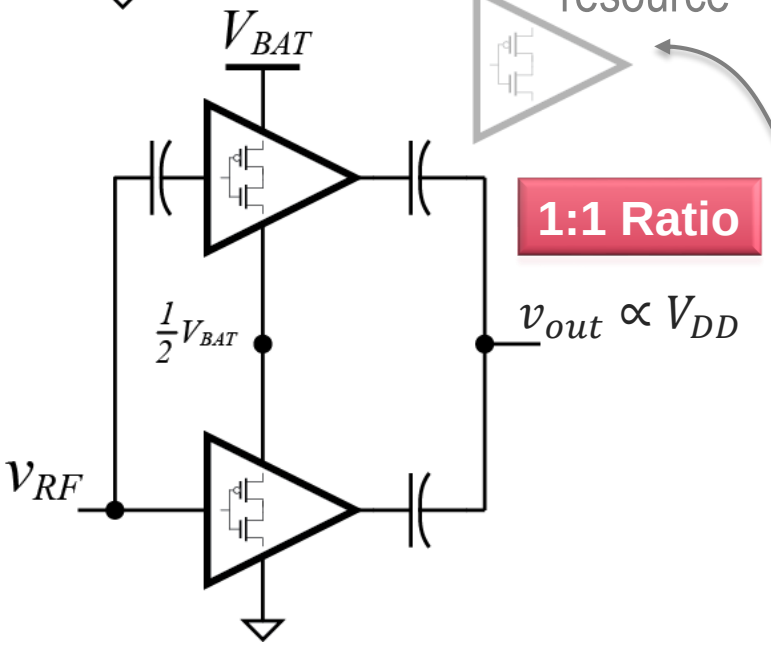
Configuring output power via ratio reconfiguration



1:2 Ratio

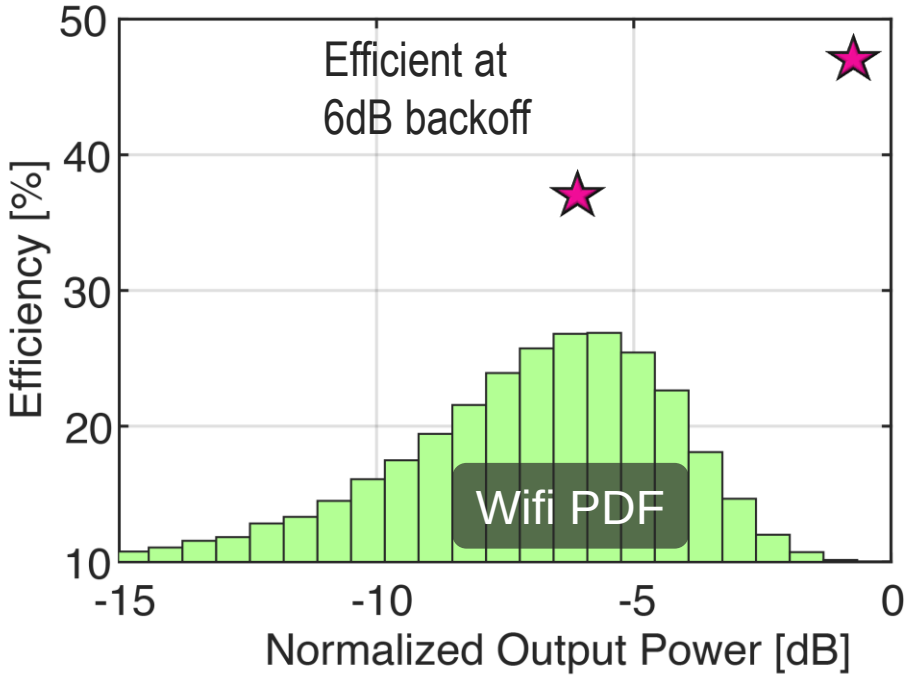
$v_{out} \propto 2V_{DD}$
$(= V_{BAT})$

Wasted resource



1:1 Ratio

$v_{out} \propto V_{DD}$



Problem: Efficiency is proportional to switch width & capacitor size

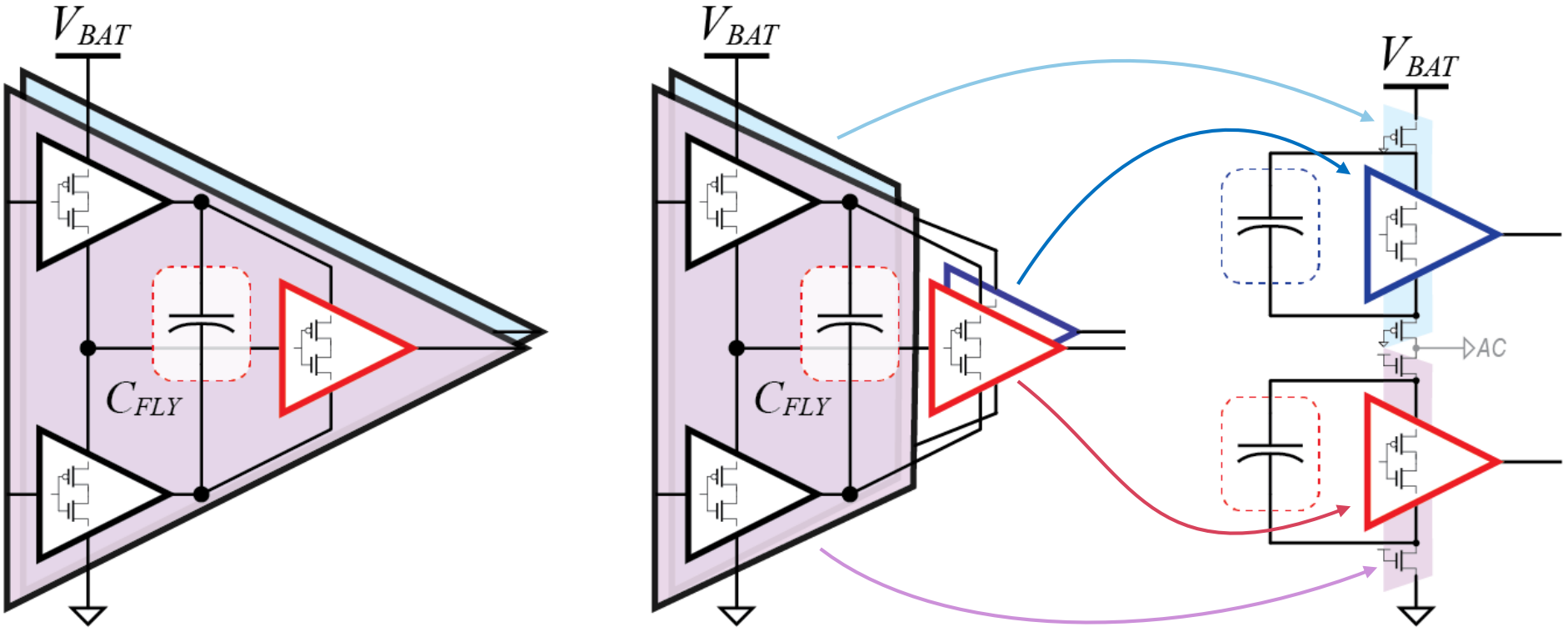
Question: How to reconfigure while utilizing all available on-chip resources?

Recursive House-of-Cards Reconfiguration

Split 1:2 HoC ratio into two cells

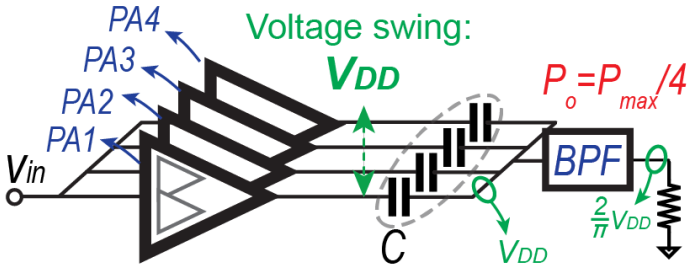
Slice into pre-driver and driver PA stages

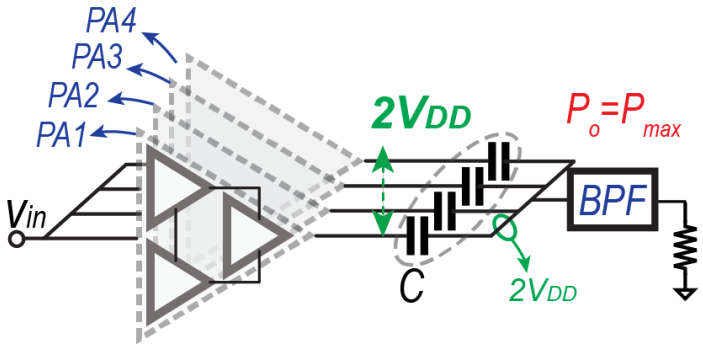
Statically-enable pre-driver stages for 1:1 ratio

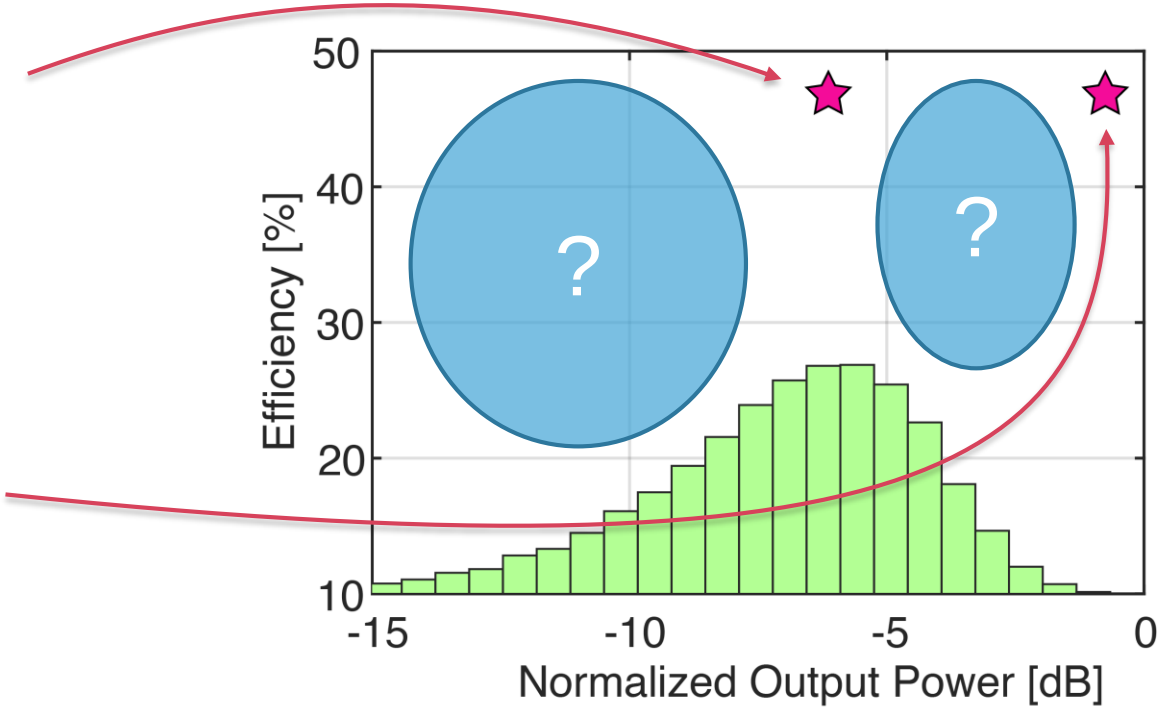


Unfolding recursive arrangement ensures 100% utilization of on-chip resources and constant R_{out} for high efficiency and linearity

Expanding output resolution via a voltage-mode λ/4-less Doherty Architecture

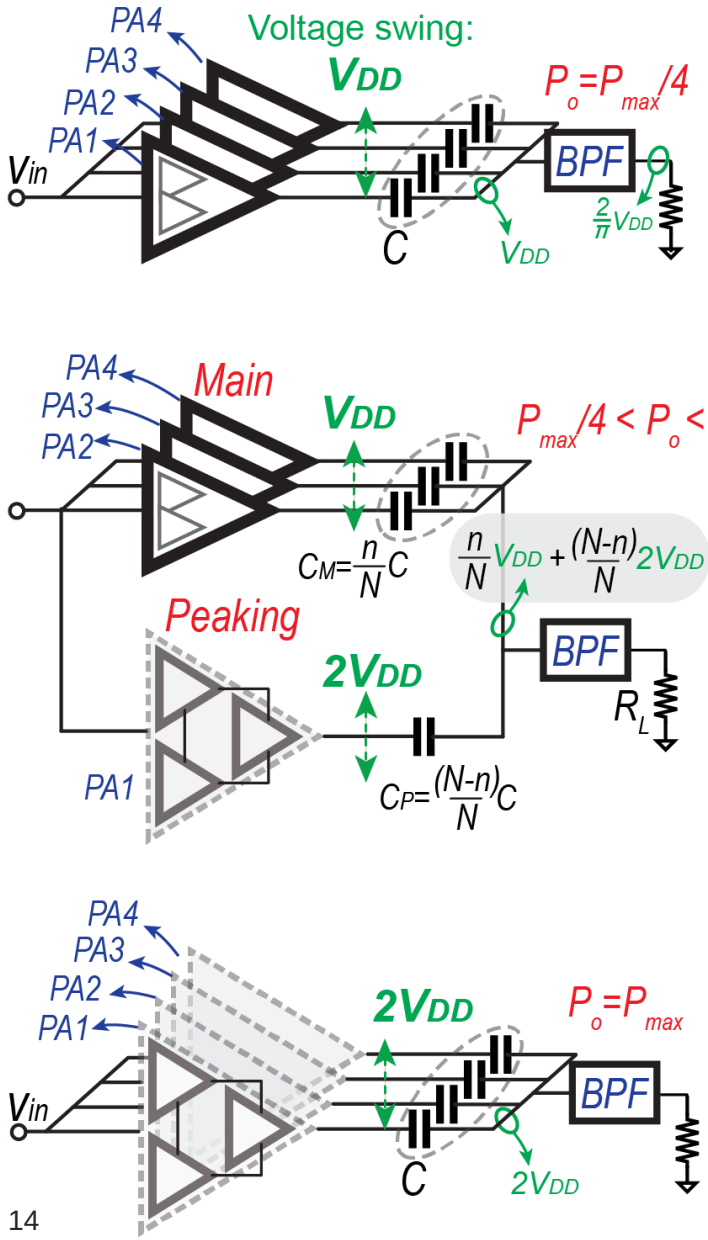


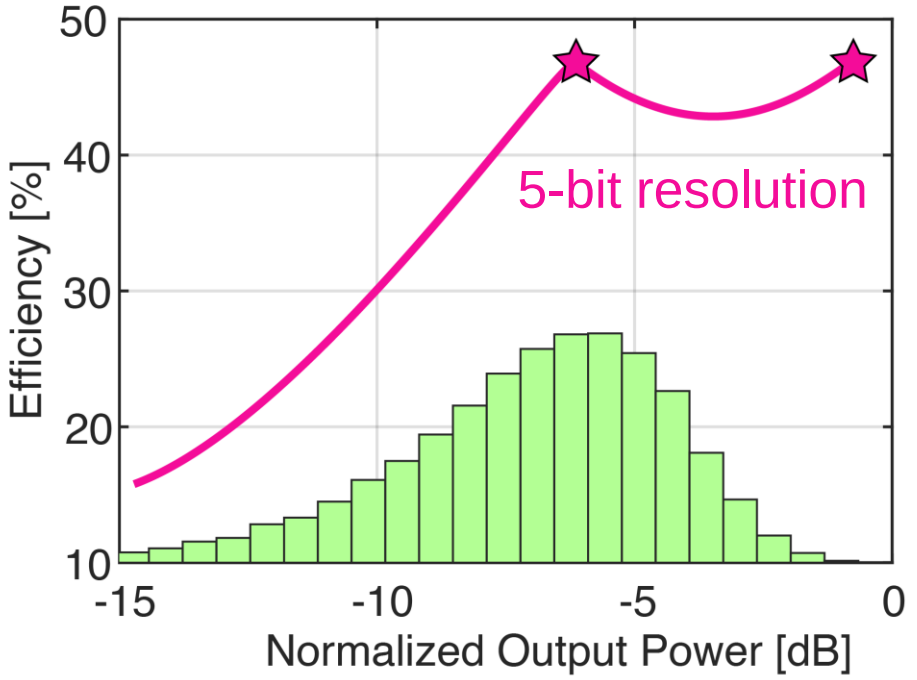




Need to generate power between ratios

Expanding output resolution via a voltage-mode λ/4-less Doherty Architecture



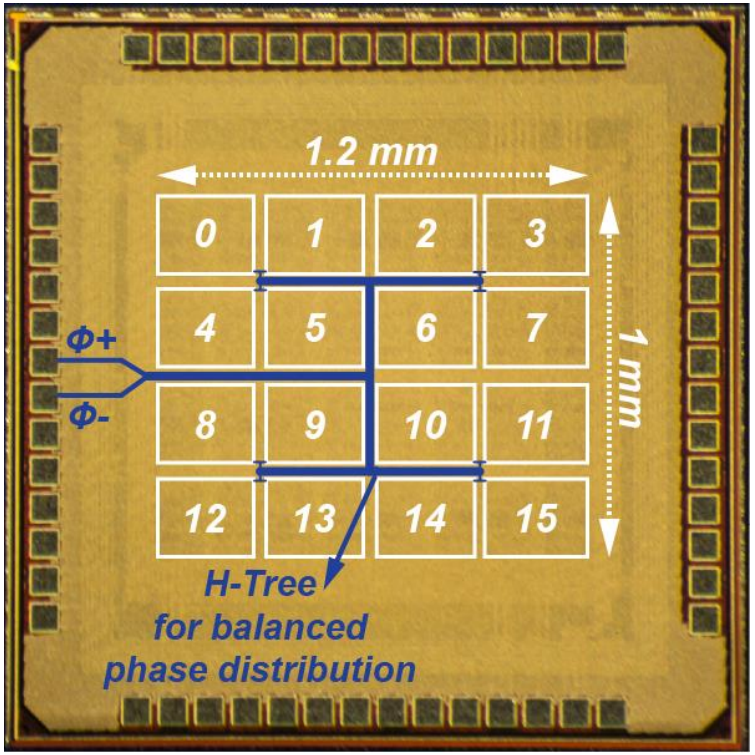


λ/4-less Doherty: power combining performed capacitively – no lossy/bulky transmission line

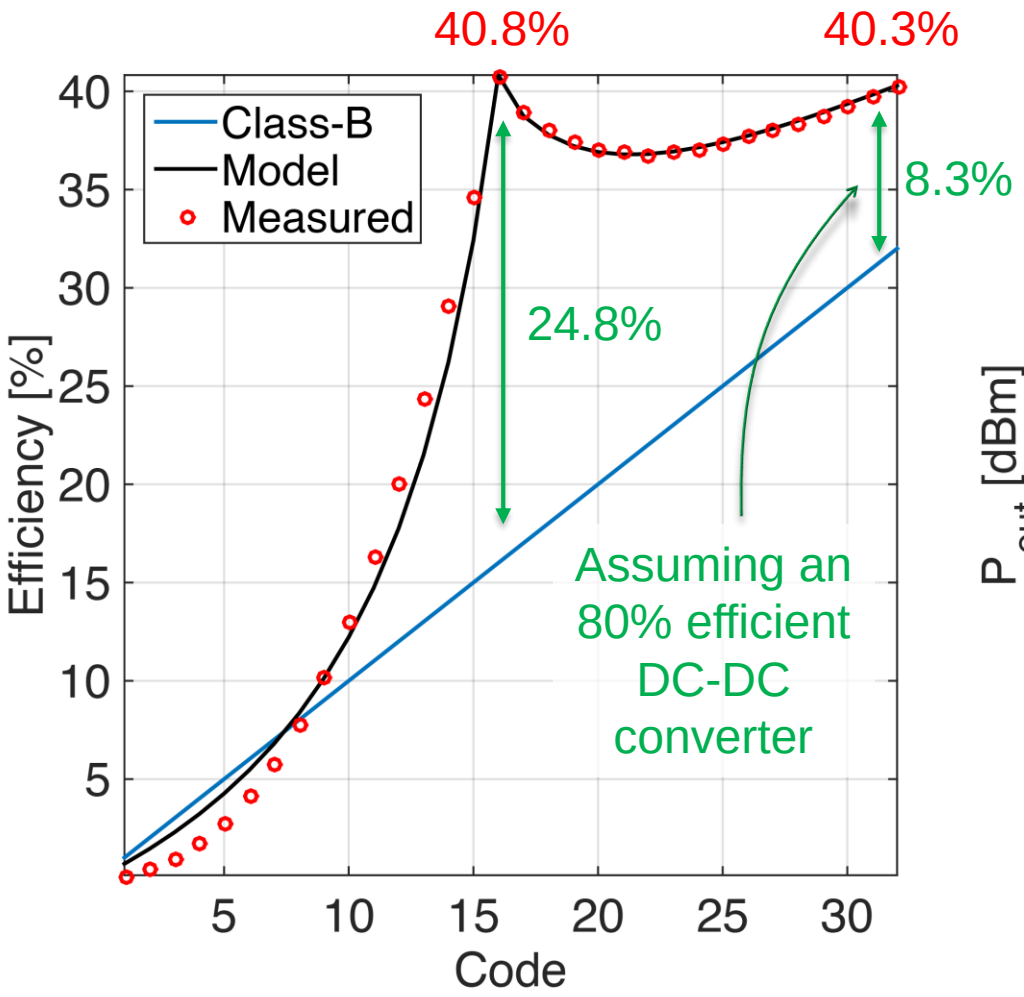
"Swapping" Doherty: unlike classic Doherty, here all PA cells are always on in the main or peaking paths, ensuring 100% resource utilization and ∴ high efficiency

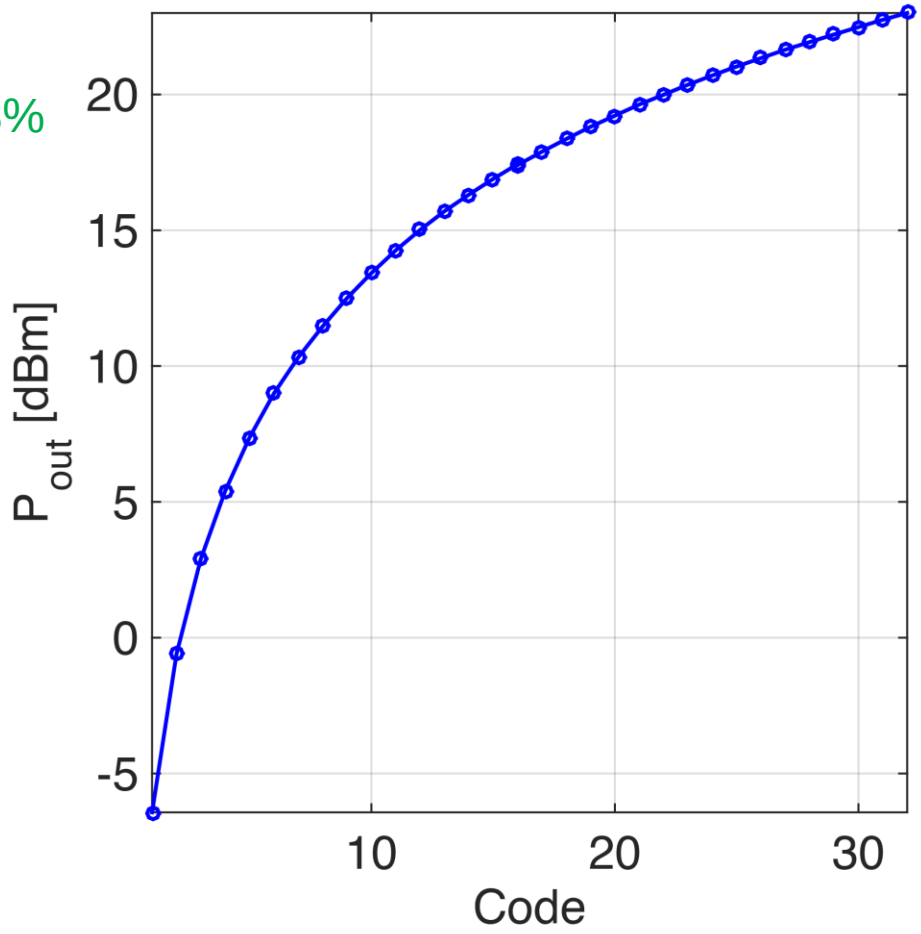
Implementation Details

Chip summary	
Process	65nm LP
Transistor voltage	1.2V
Supply voltage	4.8V Li-ion battery
Carrier frequency	Up to 1GHz
Output power	Up to 23dBm
Output resolution	5-bits
Core Area	1.2mm^2



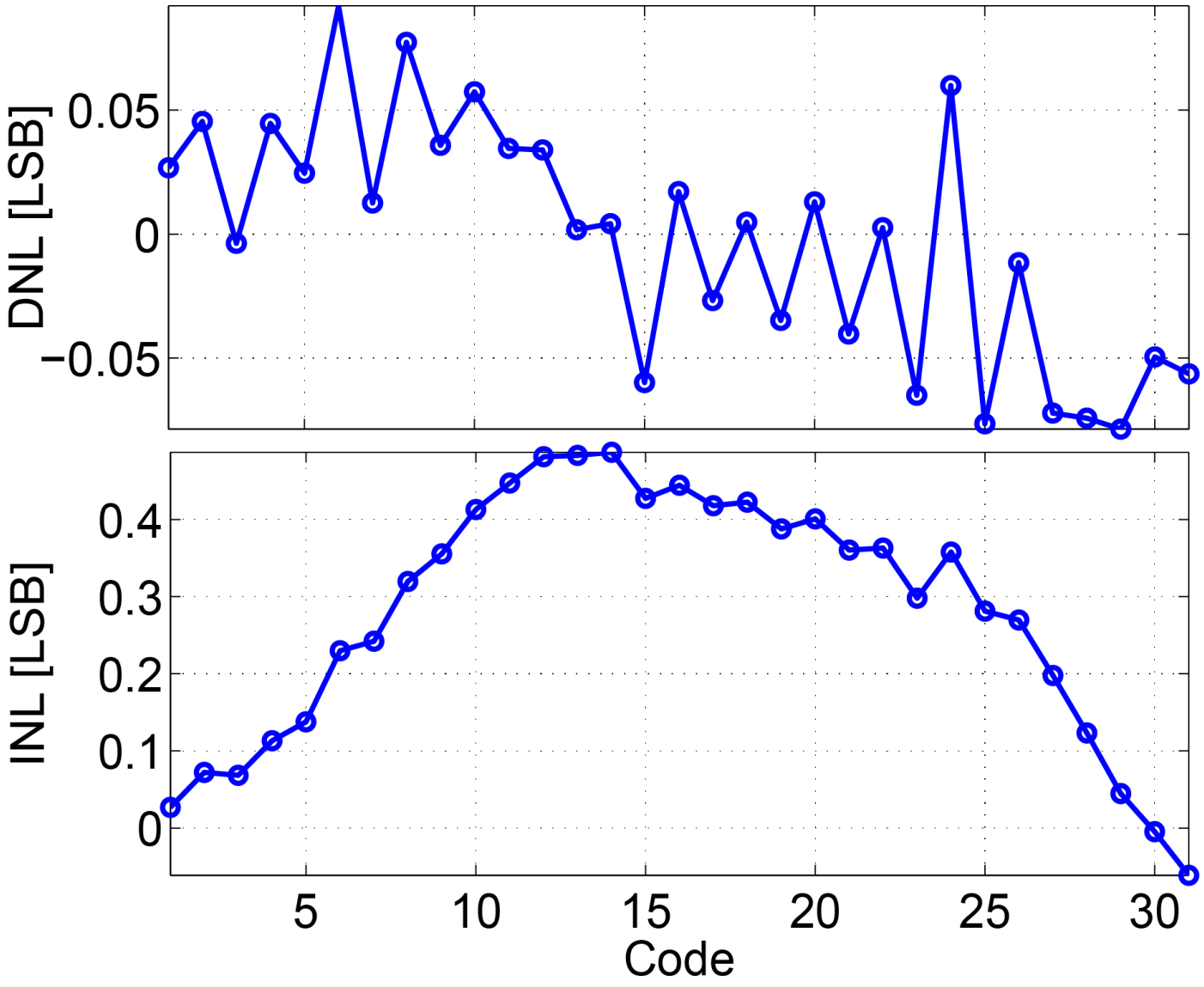
Measurement results: PAE





>40% battery-to-RF power-added efficiency at both peak power (23dBm) and at 6dB backoff

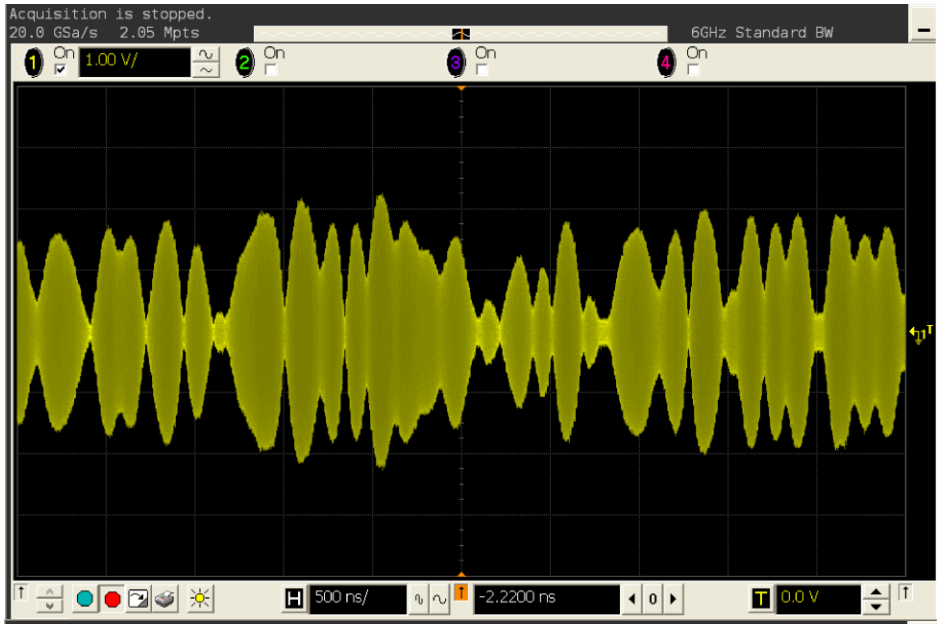
Measurement results: static linearity

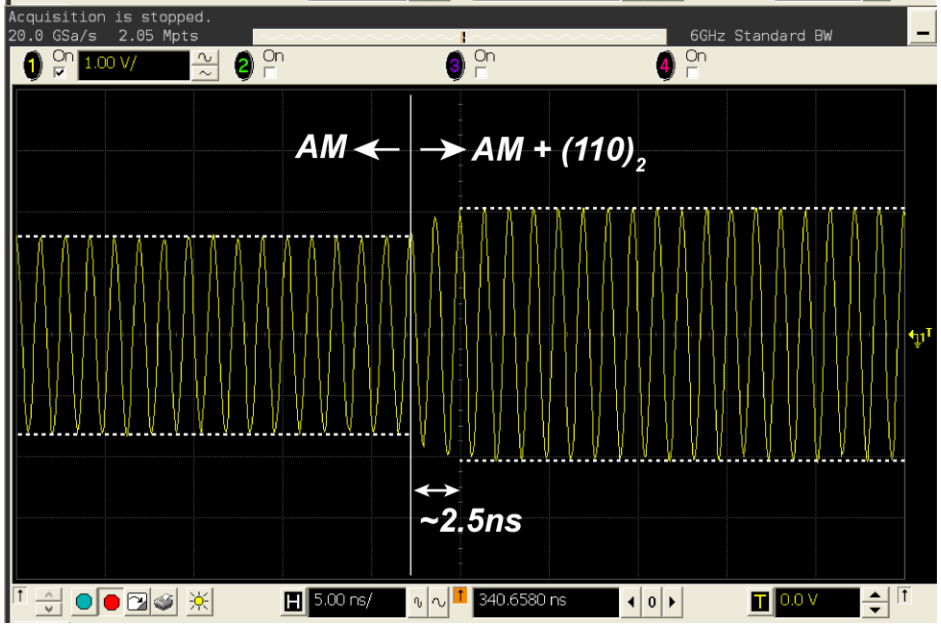


Less than 0.09 LSB

Less than 0.5 LSB

Measured output waveforms





- 32-QAM OFDM signal with 20MHz bandwidth
- Amplitude sampling rate: 100MHz
- PAPR: 7.5dB
- Average battery-to-RF efficiency: 26.2%
- 2.5ns response time for 3-bit AM code change
  - → upwards of 400MHz envelope signal
- Dynamic spectrum results coming soon (equipment has been ordered)

Conclusions

- **Research challenge:** Difficult to design conventional linear PAs in scaled CMOS; power combining approaches have cascaded losses
- **Proposed solution:** a Recursive House-of-Cards topology that stacks class-D PA cells to generate large amplitude RF waveforms directly from a battery using ~1V transistors
- **Additional techniques:** a λ/4-less Doherty power combiner that utilizes 100% of on-chip resources to efficiently create 5-bits of resolution
- **Results:** a 65nm LP test chip that delivers >40% PAE at both 23dBm and 6dB back-off with an envelope rate up to 400MHz

Acknowledgement: DARPA grant D15AP00091