An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range

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Parallelism, The Way For Higher Processing

- Higher-frequency exceeds thermal limits

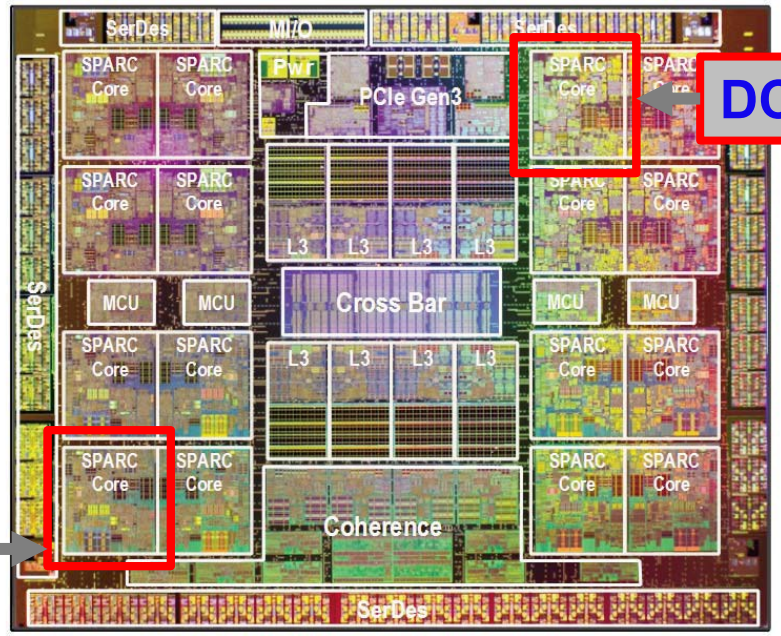
High performance & low power:
- Parallel processing (multi-core)

No. of processing engines exponentially increases to meet customer expectations

ITRS

Per-module voltage scaling for adapting power with processing load

Fully-integrated DC-DC Converters are required



T5 SPARC, 16 Core, ISSCC'13

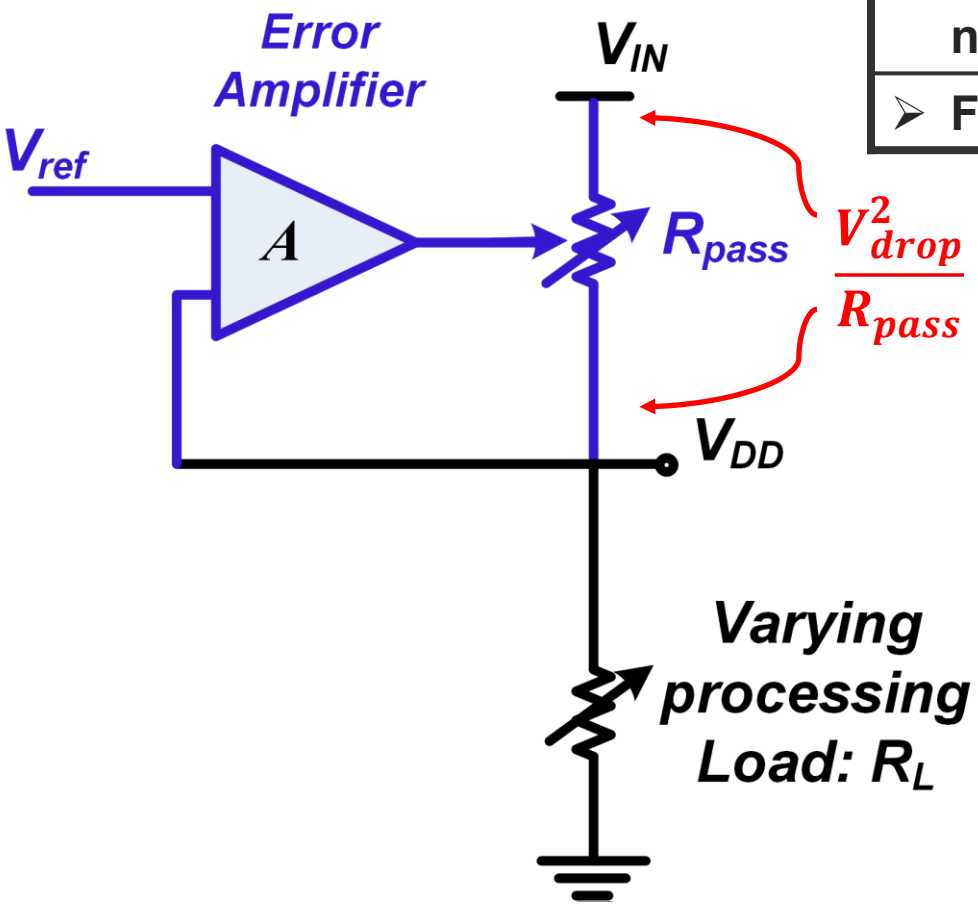
Outline

- On-Die DC-DC Converters
- Recursive SC Topology
- All Digital Binary Search Control
- Measurement Results
- Conclusions

Linear Voltage Regulator

- A resistive divider

➢ Compact ➢ No switching noise ➢ Fast	➢ Very lossy when V_{DD} goes far below V_{IN}

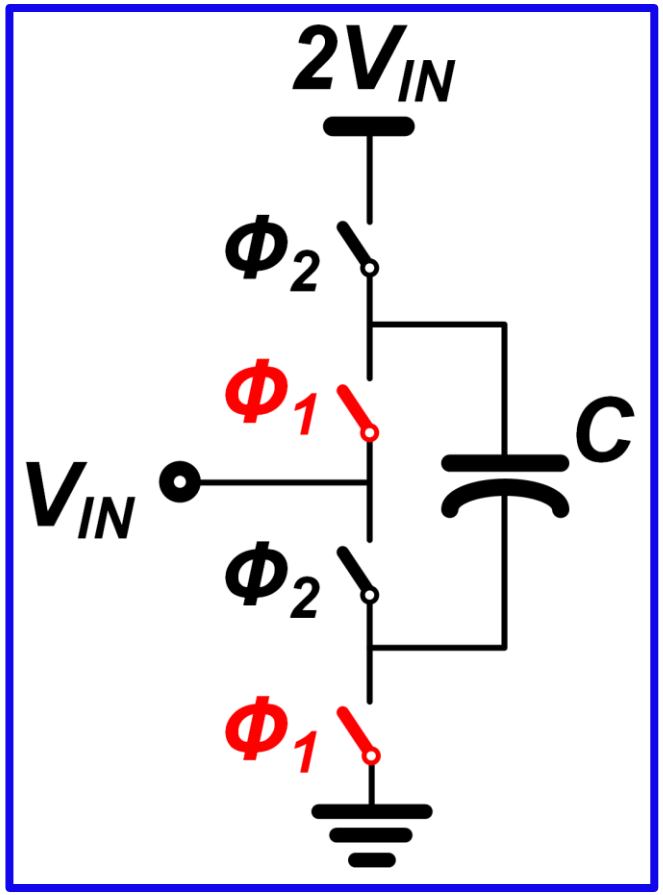


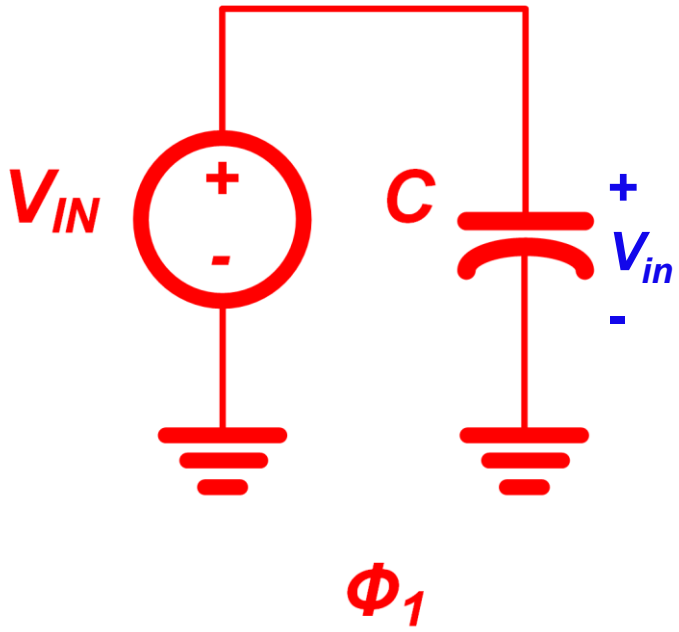
$$\eta = \frac{V_{DD}}{V_{IN}}$$

Switched Capacitor DC-DC Converters

- How to convert input DC voltage?

Switched Capacitor





Switched Capacitor DC-DC Converters

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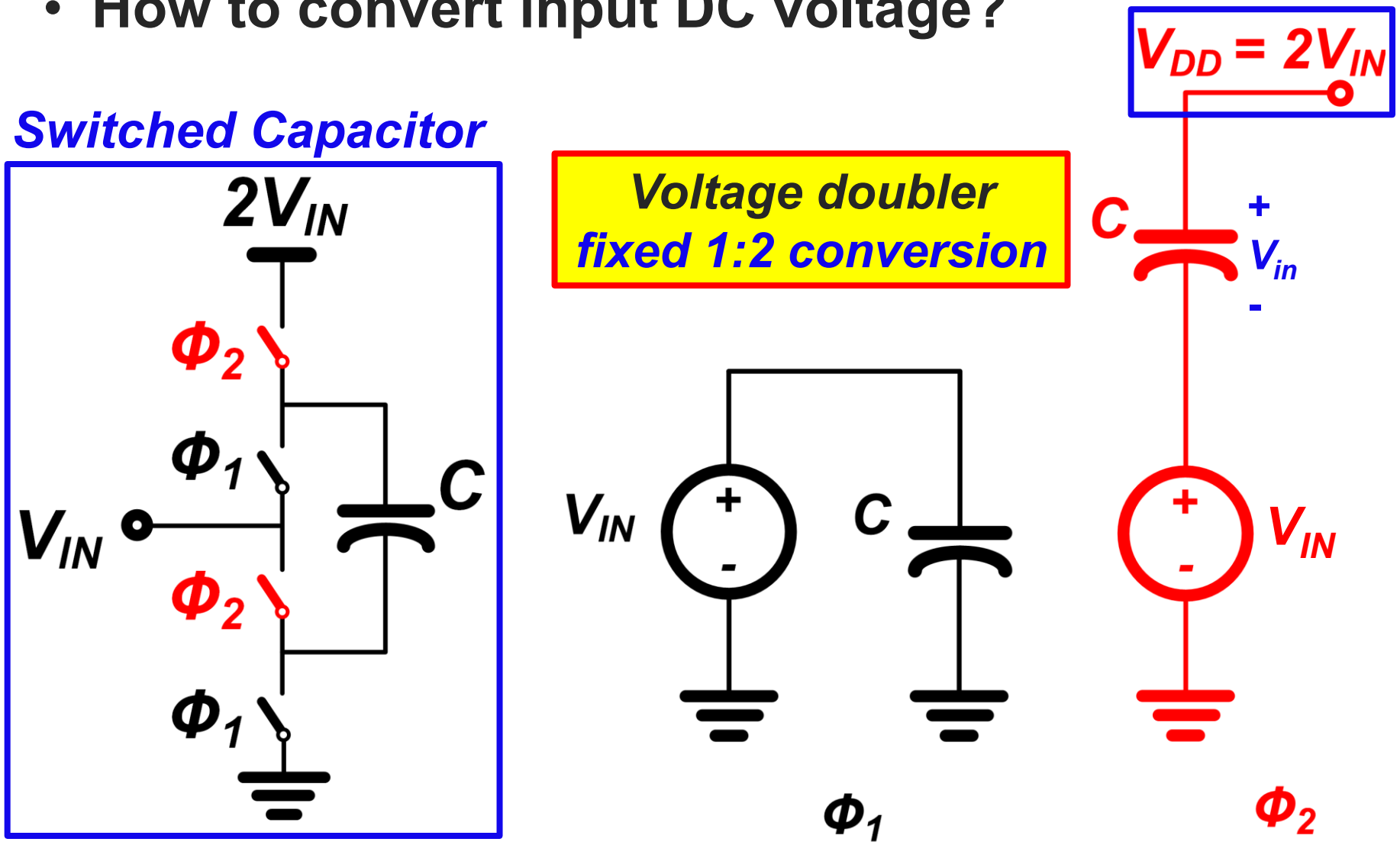

Switched Capacitor DC-DC Converters

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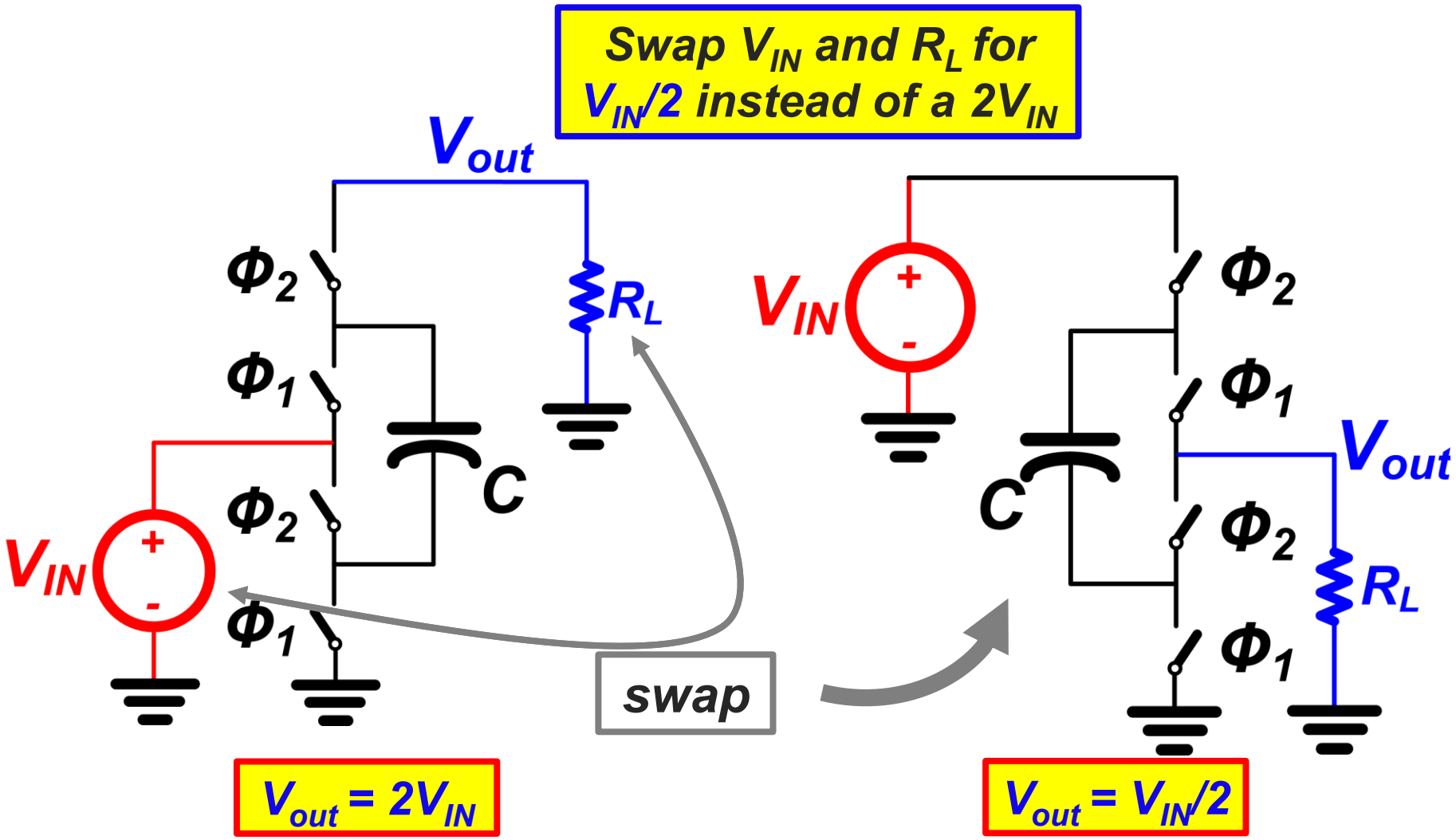
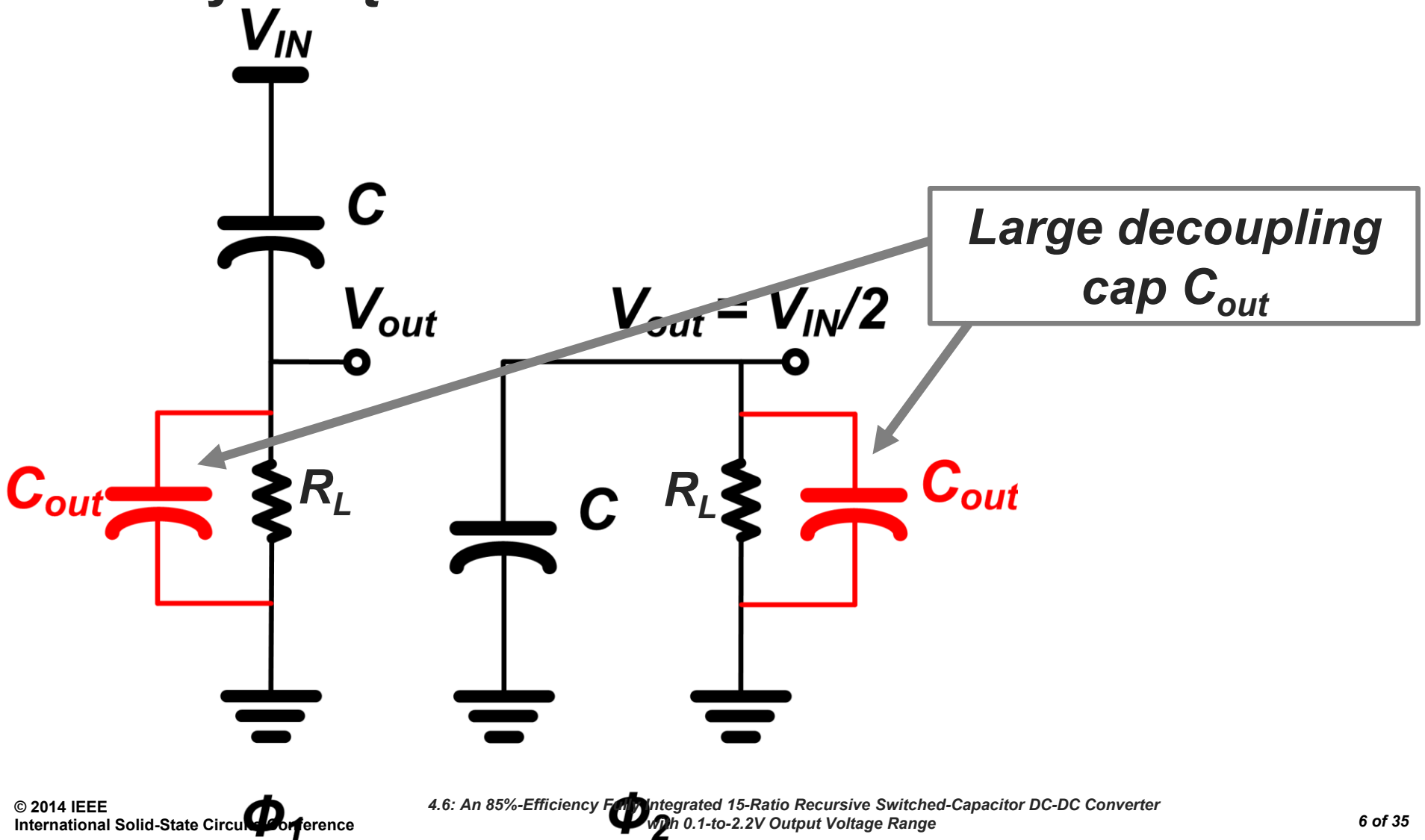


SC Loss

- Why *SC* $\eta \neq 100\%$?



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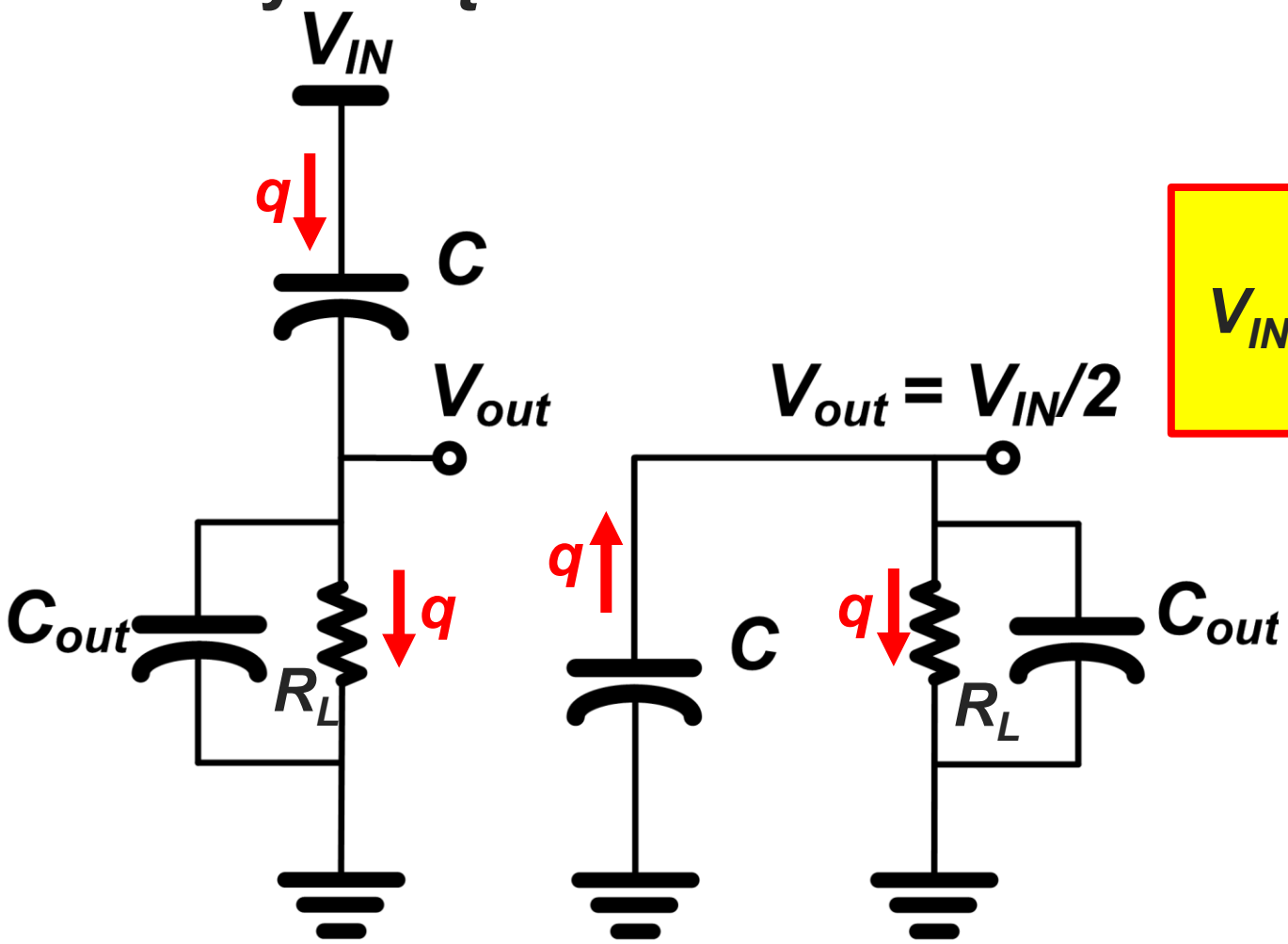
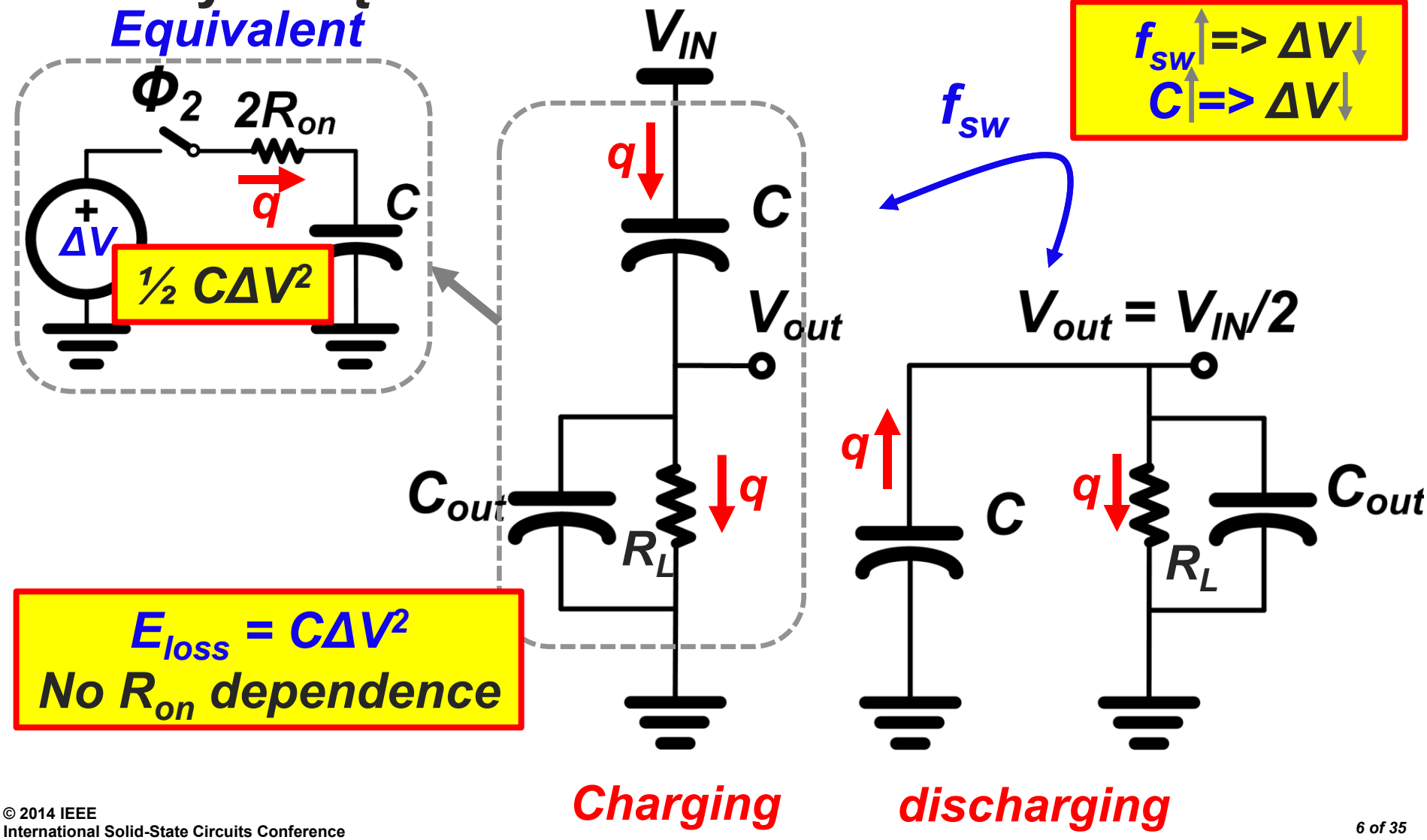


$q_{out} = 2q$
$V_{IN}\ q = V_{IN}/2\ 2q$
$E_{in} = E_{out}$

Charging discharging

SC Loss

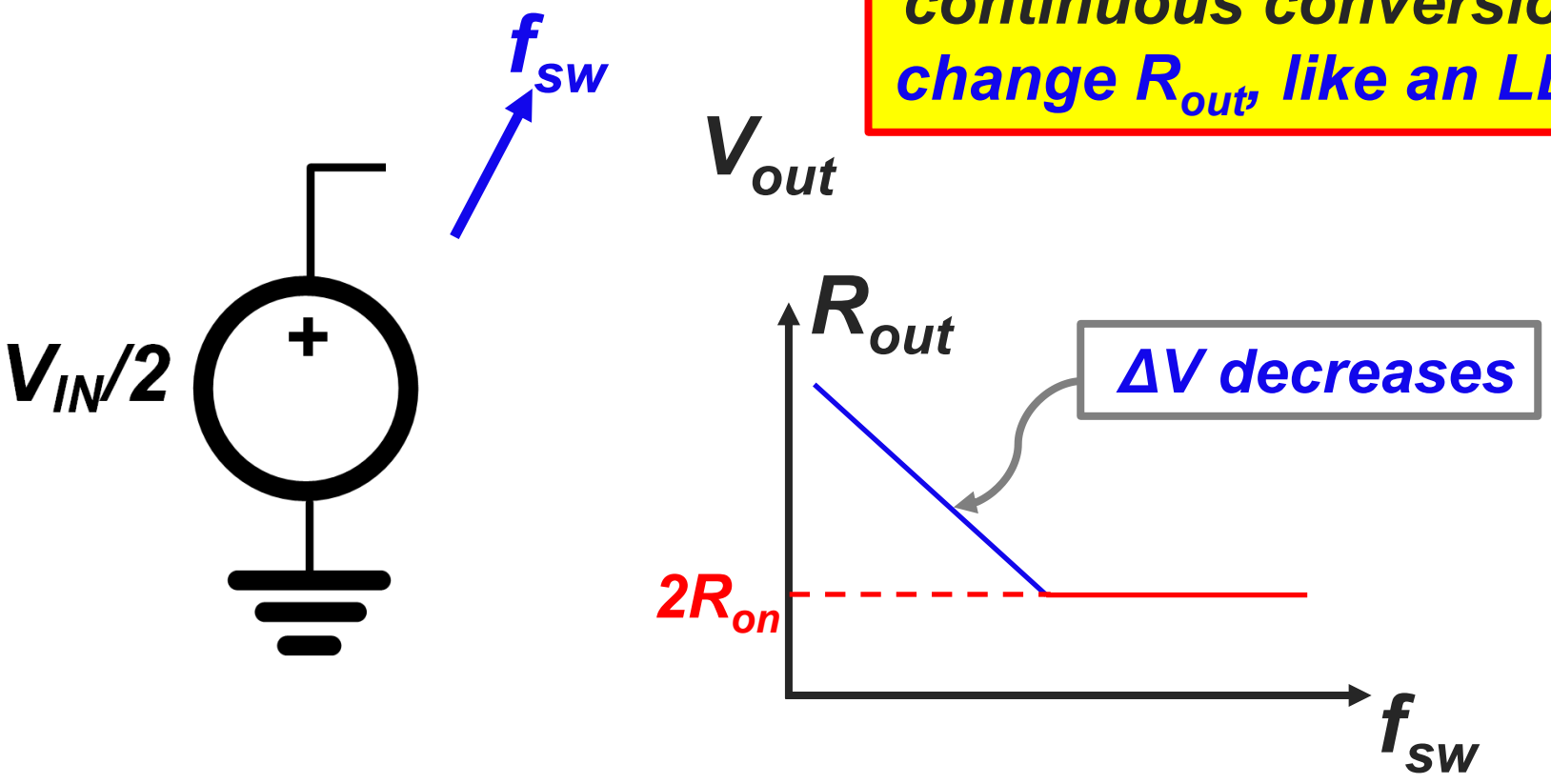
- Why *SC* $\eta \neq 100\%$?



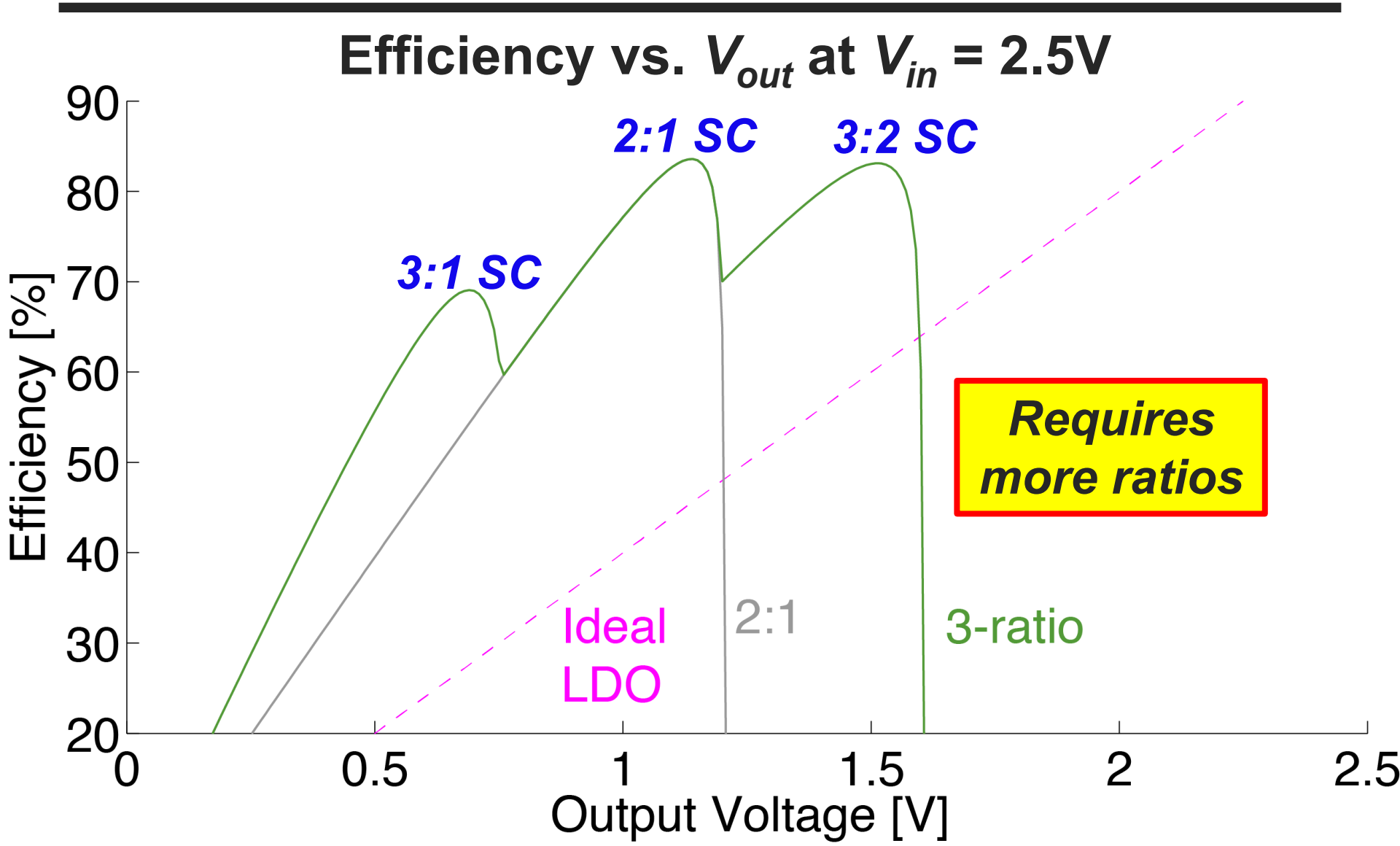
2:1 SC Model

- Loss can be modeled by R_{out}

This is how to provide continuous conversion: change R_{out}, like an LDO

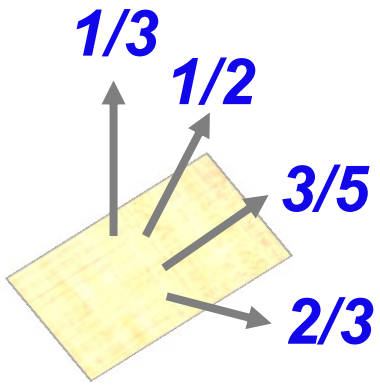


Series-Parallel SC Efficiency



Higher Number of Ratios Challenge with Conventional SC Topologies

Problem: Given certain C, re-use that to produce different ratios



- ***No. Of caps and switches increases exponentially***
- ***Each ratio requires a unique arrangement, which is difficult to re-use among other ratios***

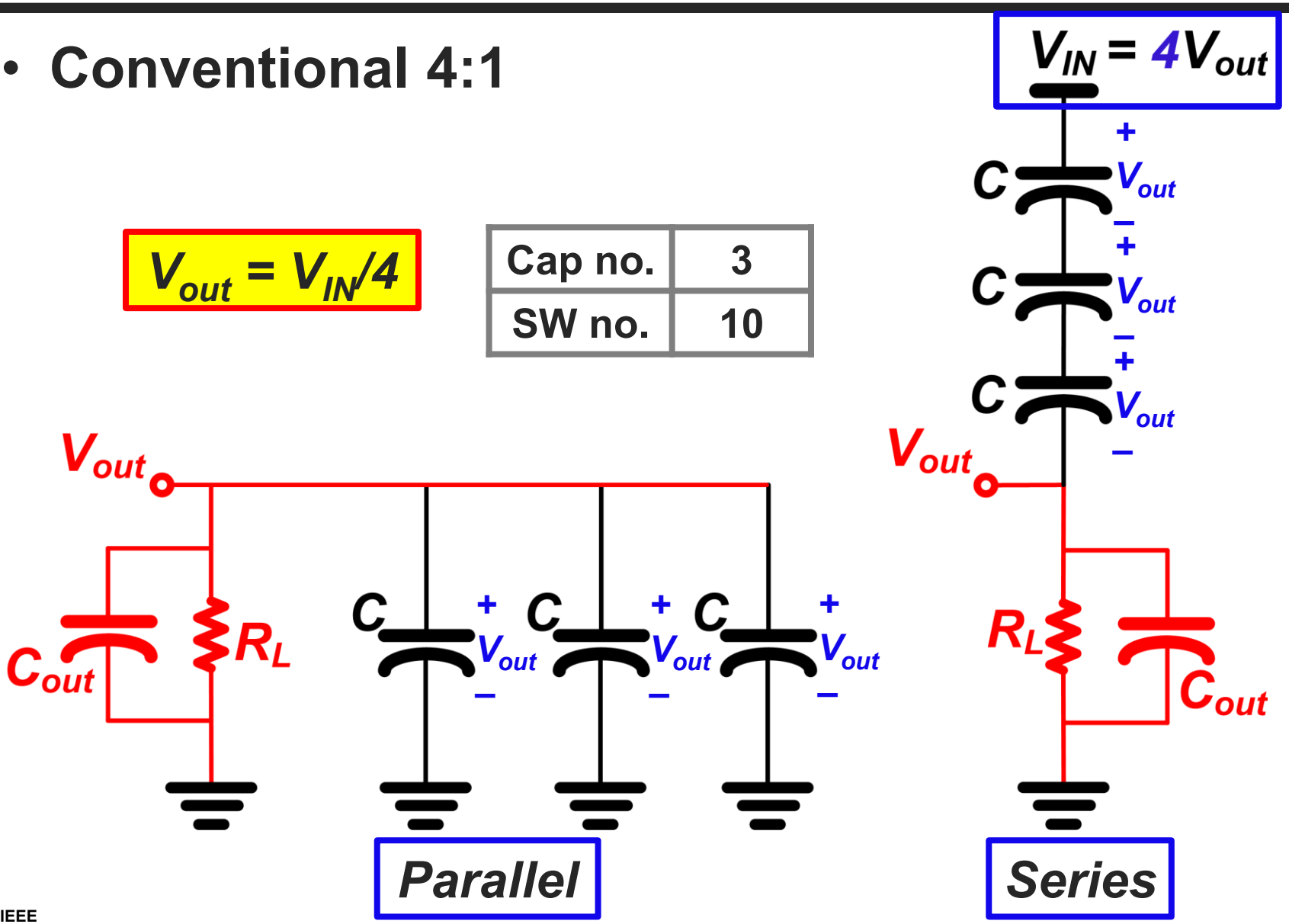
Higher no. of ratios requires a Modular topology

SC 4:1 Series-Parallel

- Conventional 4:1

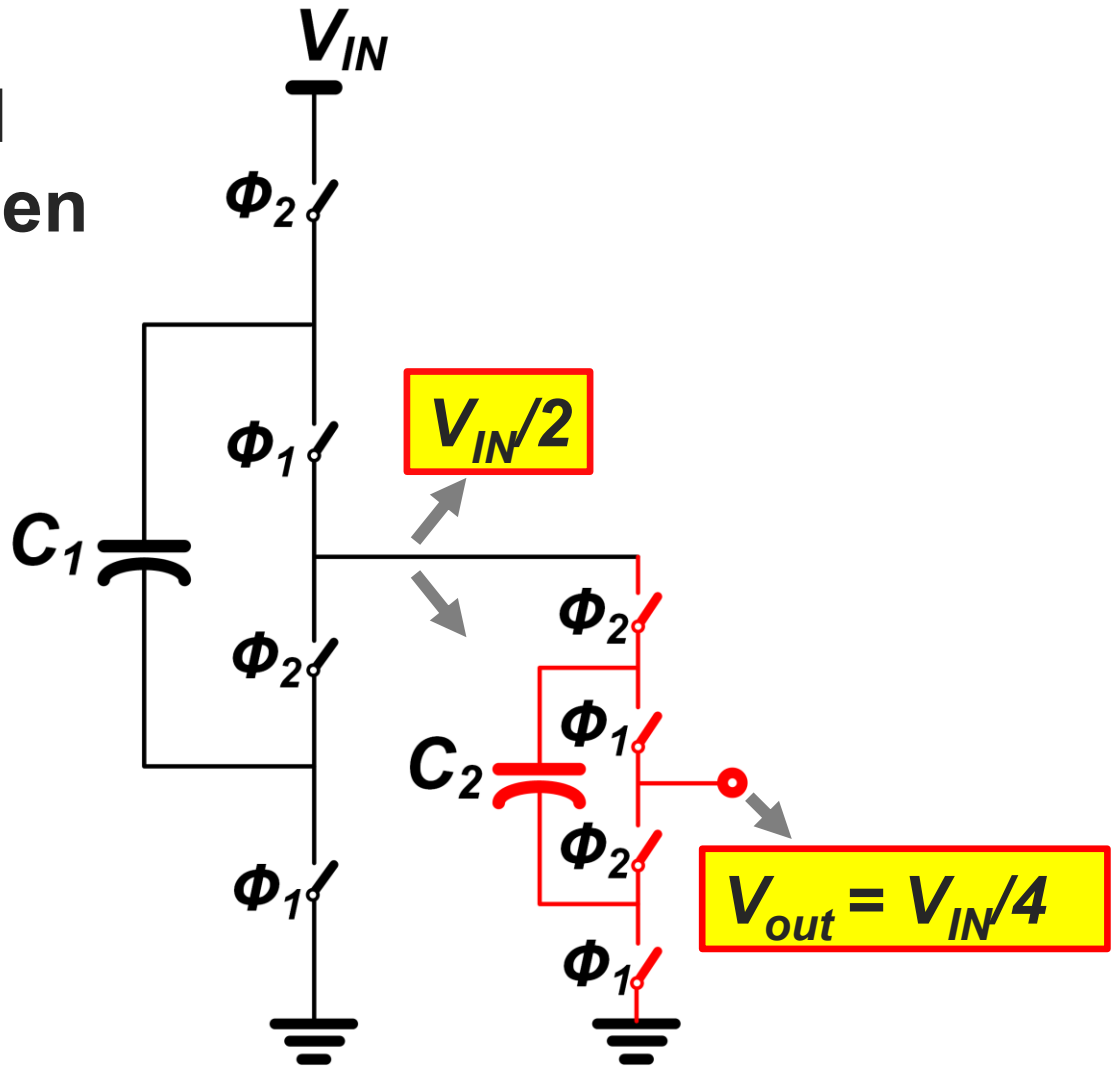
$V_{out} = V_{IN}/4$

Cap no.	3
SW no.	10



Proposed Modular Switched-Capacitor Topology

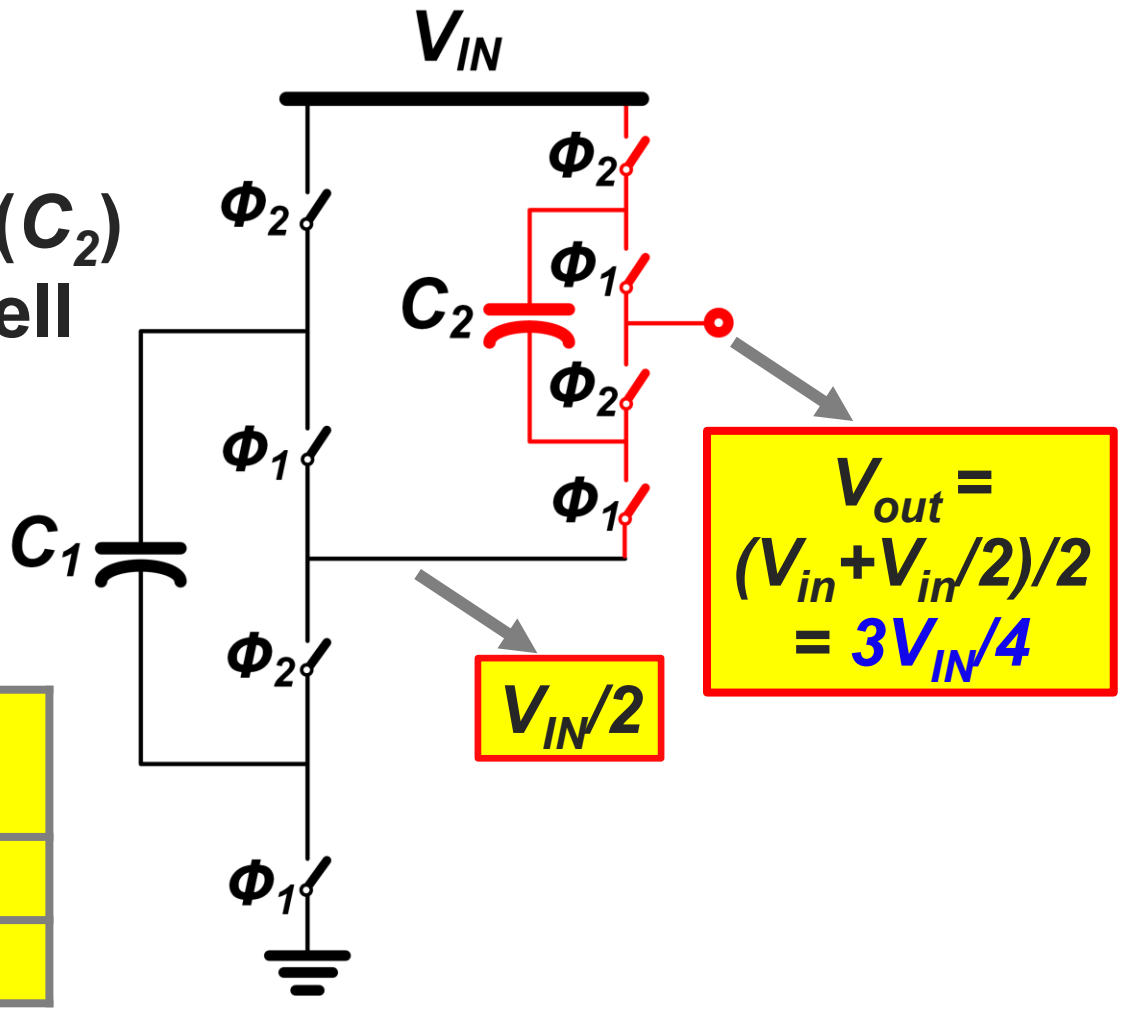
- **Ratio = 1/4**
- Connect a second 2:1 cell (C_2) between cell (C_1) output & GND



	SP 1/4	New 1/4
Cap no.	3	2
SW no.	10	8

Proposed Modular Switched-Capacitor Topology

- **Ratio = 3/4**
- Connect the second 2:1 cell (C_2) between V_{IN} & cell (C_1) output

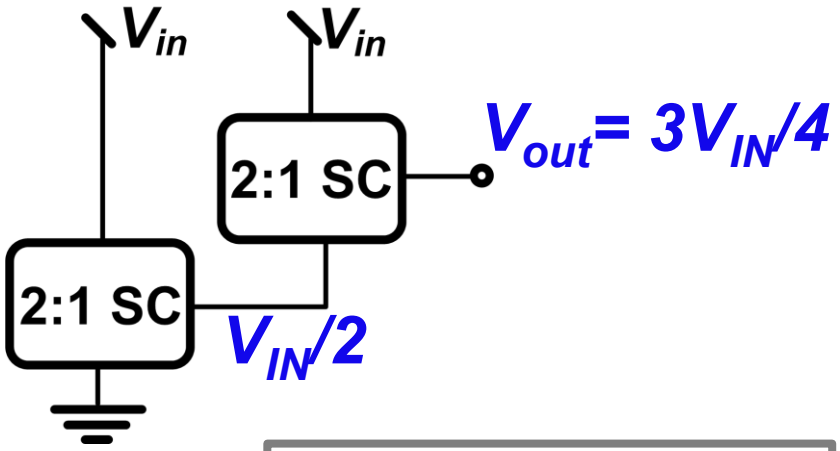


	SP 3/4	New 3/4
Cap no.	3	2
SW no.	10	8

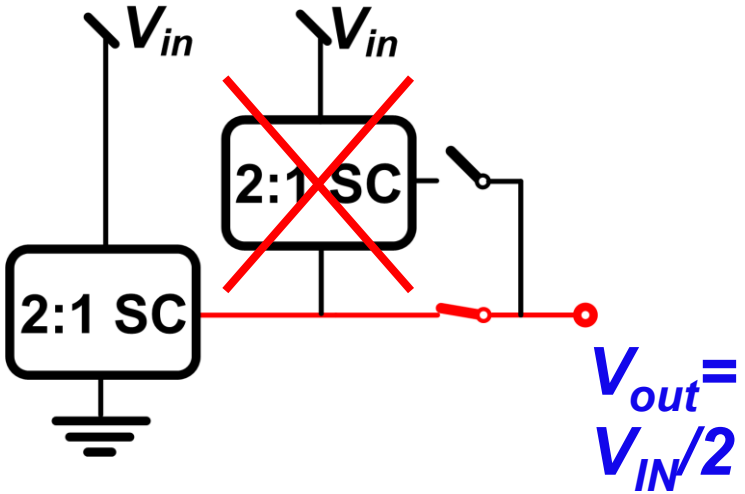
SC Ratio Reconfiguration

- 1/4, 3/4 are realized, how to get 1/2

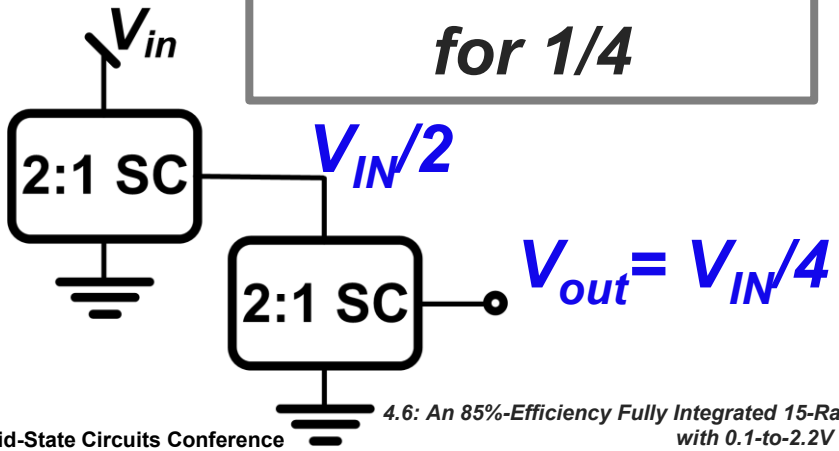
Cells Stacked for 3/4



Route V_{out} from 1st cell for 1/2



Cells cascaded for 1/4

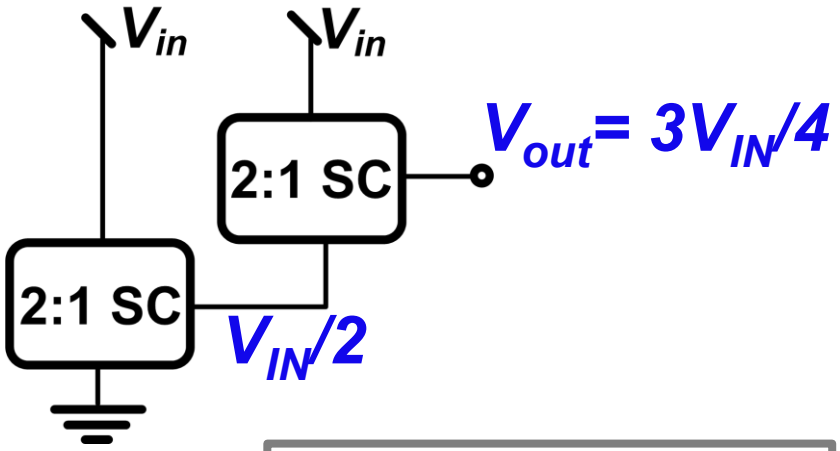


Wastes the capacitance of the 2nd cell, lower η

Recursive SC Ratio Reconfiguration

- 1/4, 3/4 are realized, how to get 1/2

Cells Stacked for 3/4



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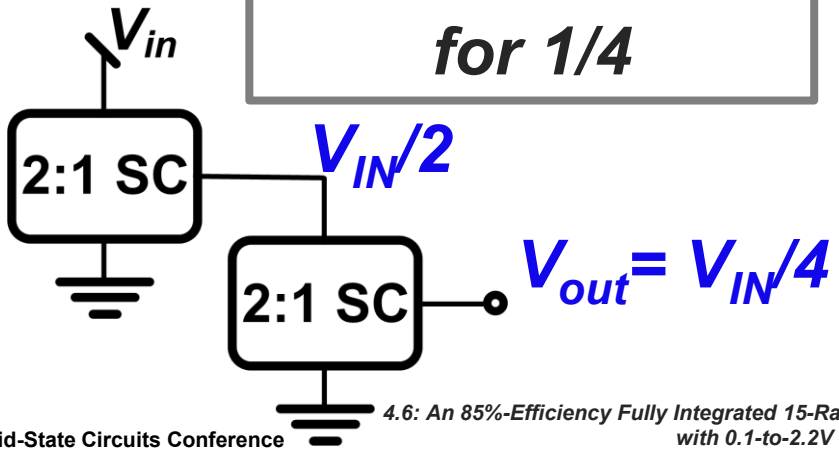
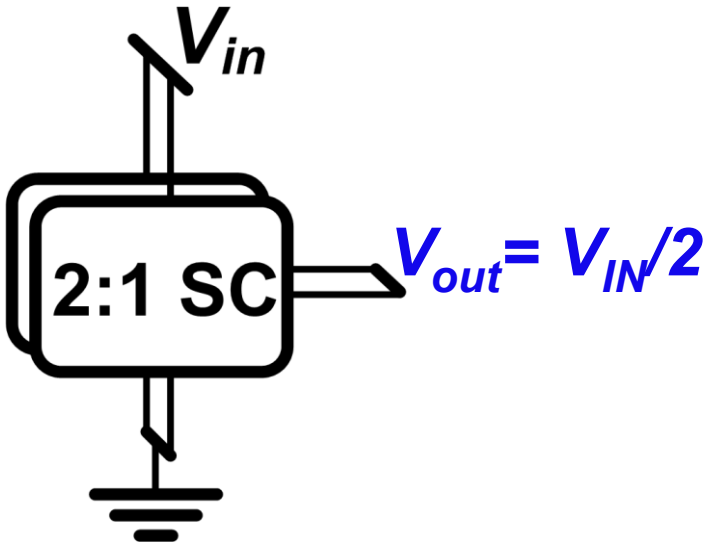


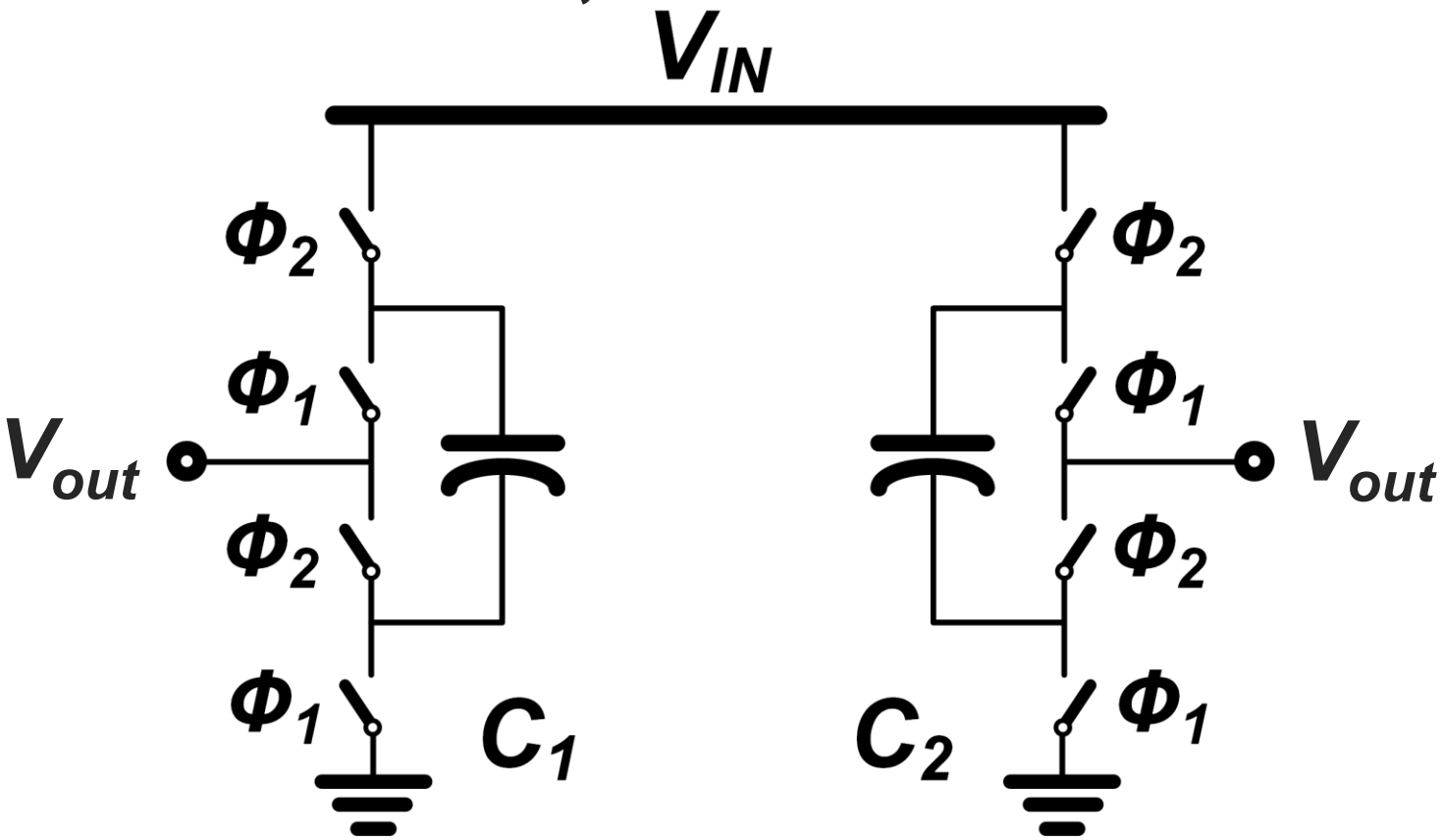
Cells in parallel for 1/2



***Recursive Inter-cell Connection*:100% of the Caps used among all ratios**

Recursive Inter-Cell Connection

- How to realize 1/2, the switch detail



Ratio = 1/2
two cells in parallel

Recursive Inter-Cell Connection

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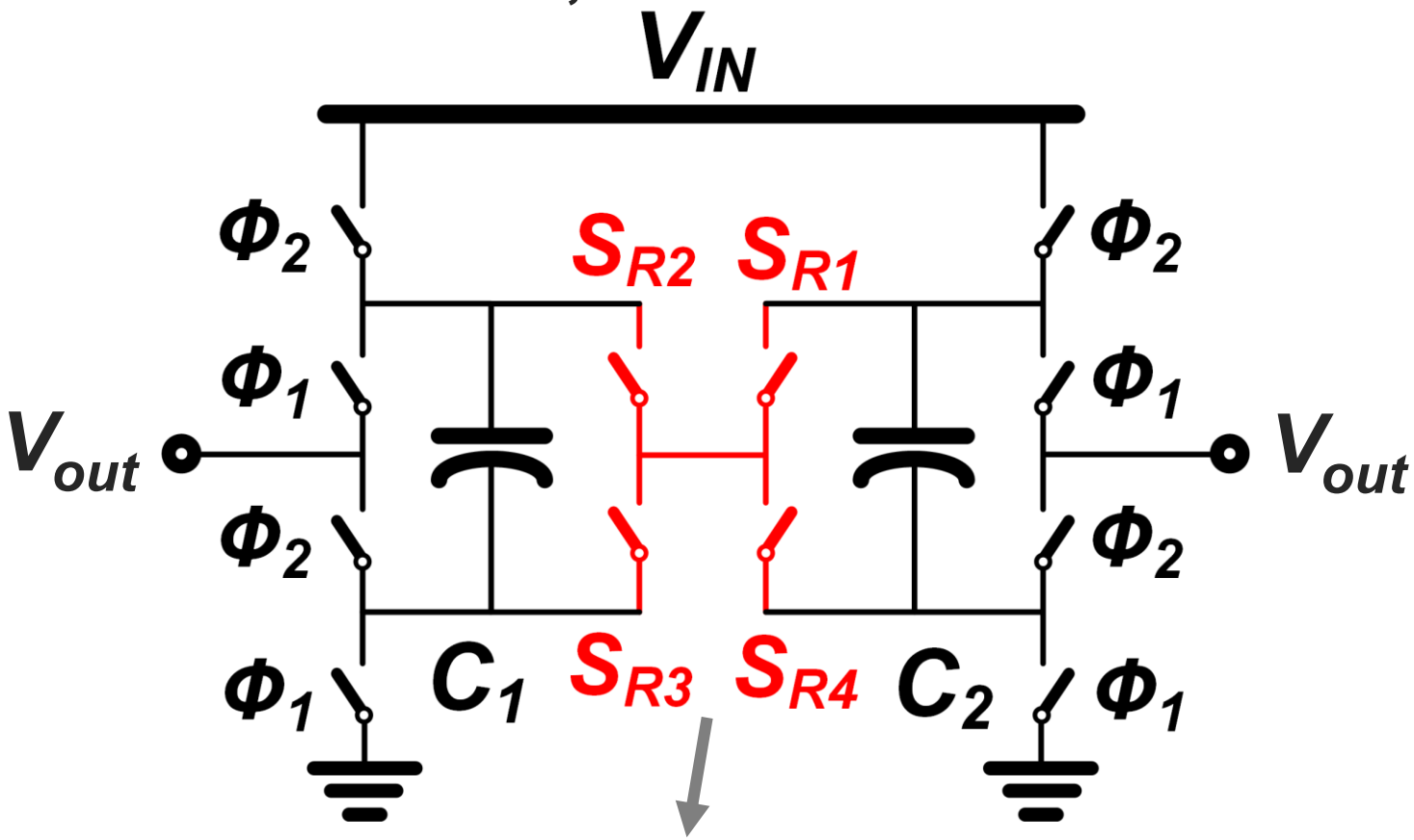

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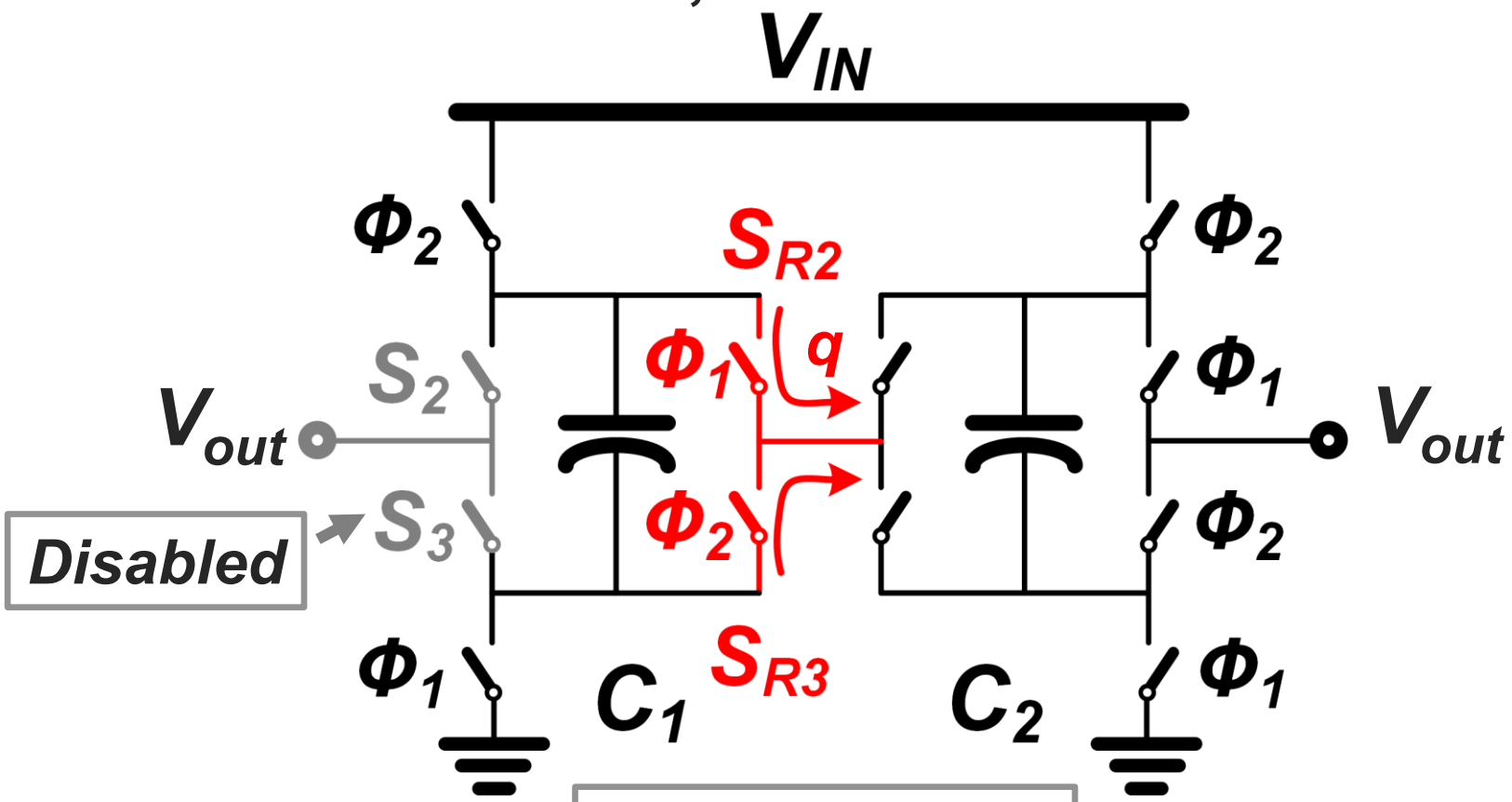
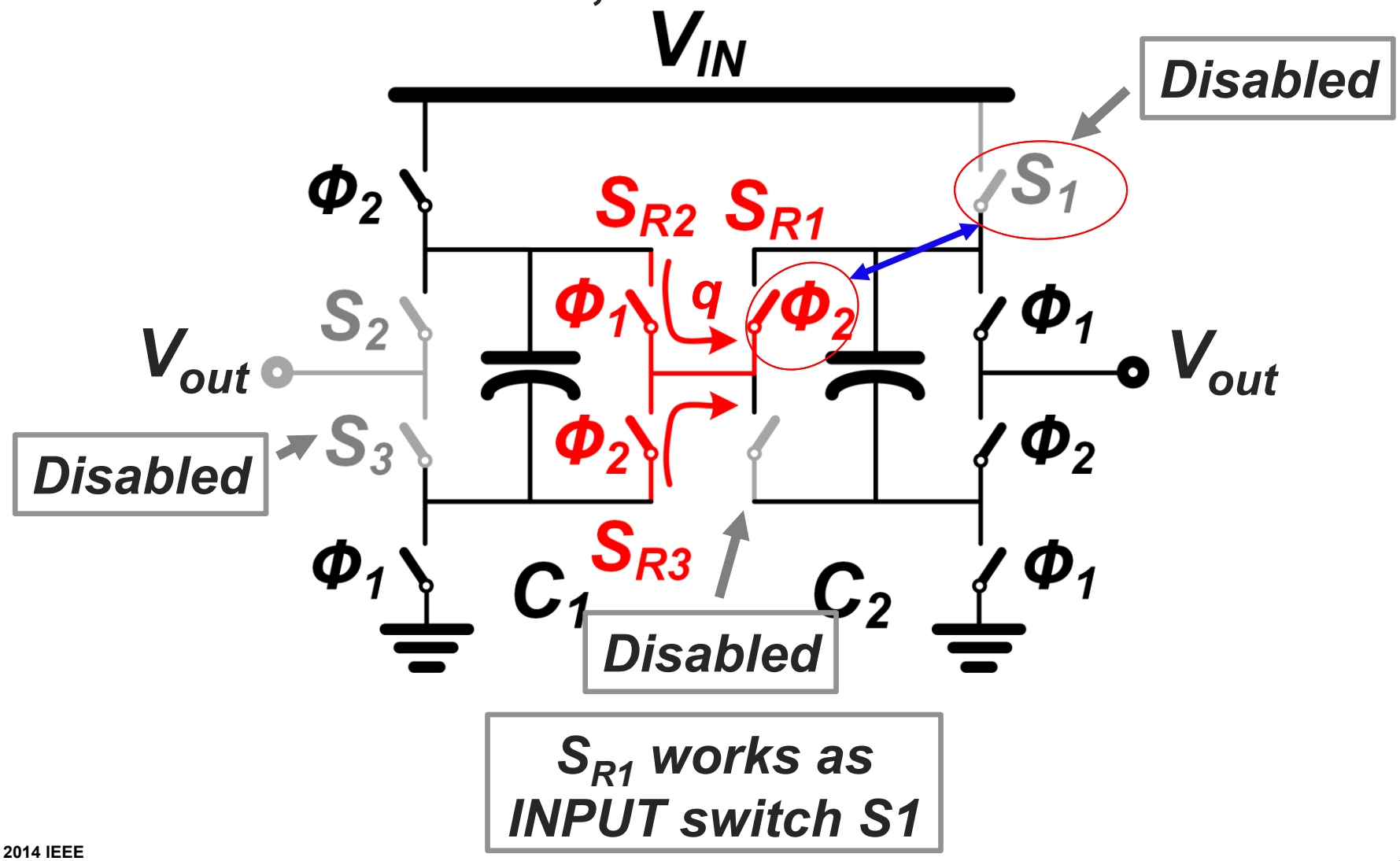


S_{R2} & S_{R3} work as OUTPUT switches

Recursive Inter-Cell Connection

- How to realize 1/4, the switch detail



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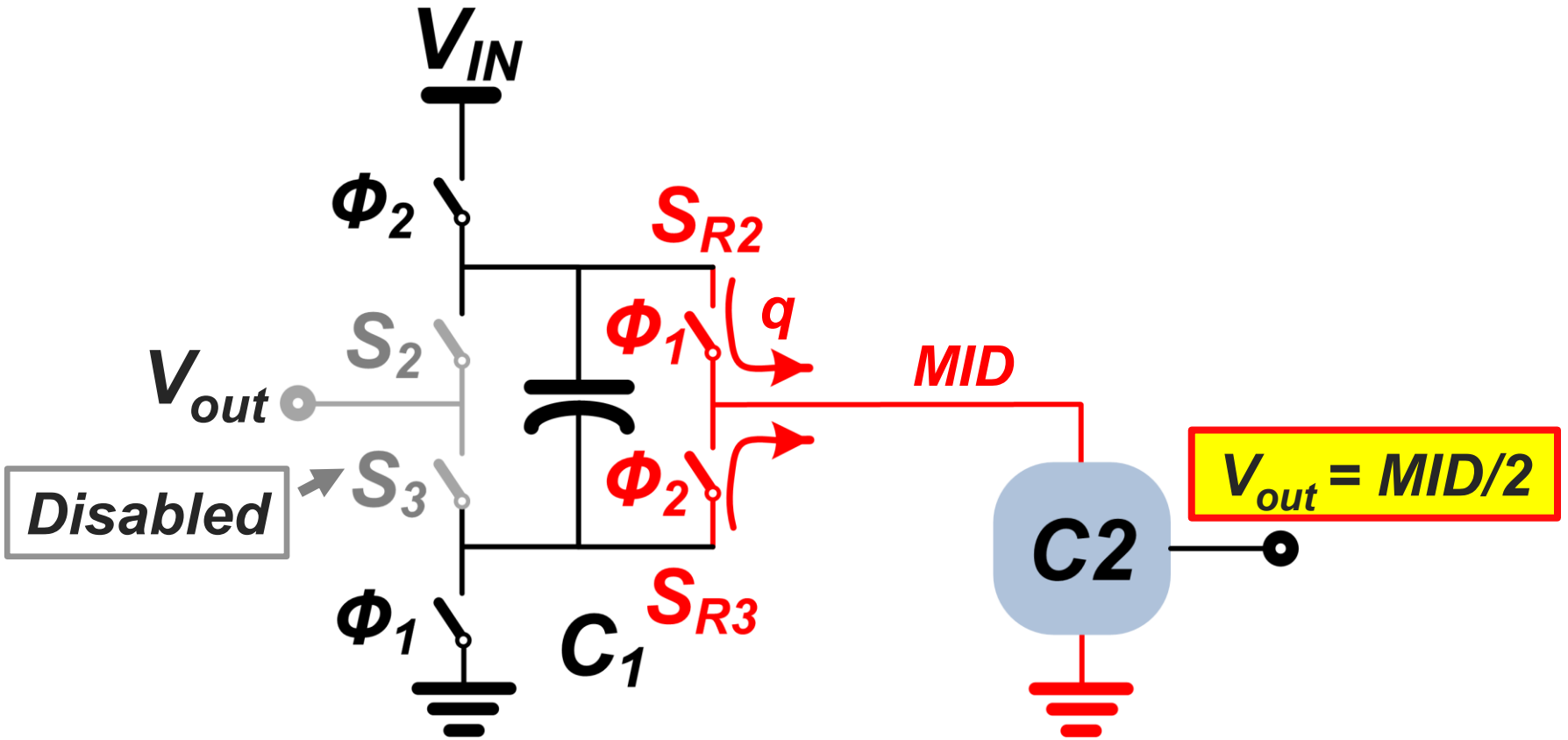
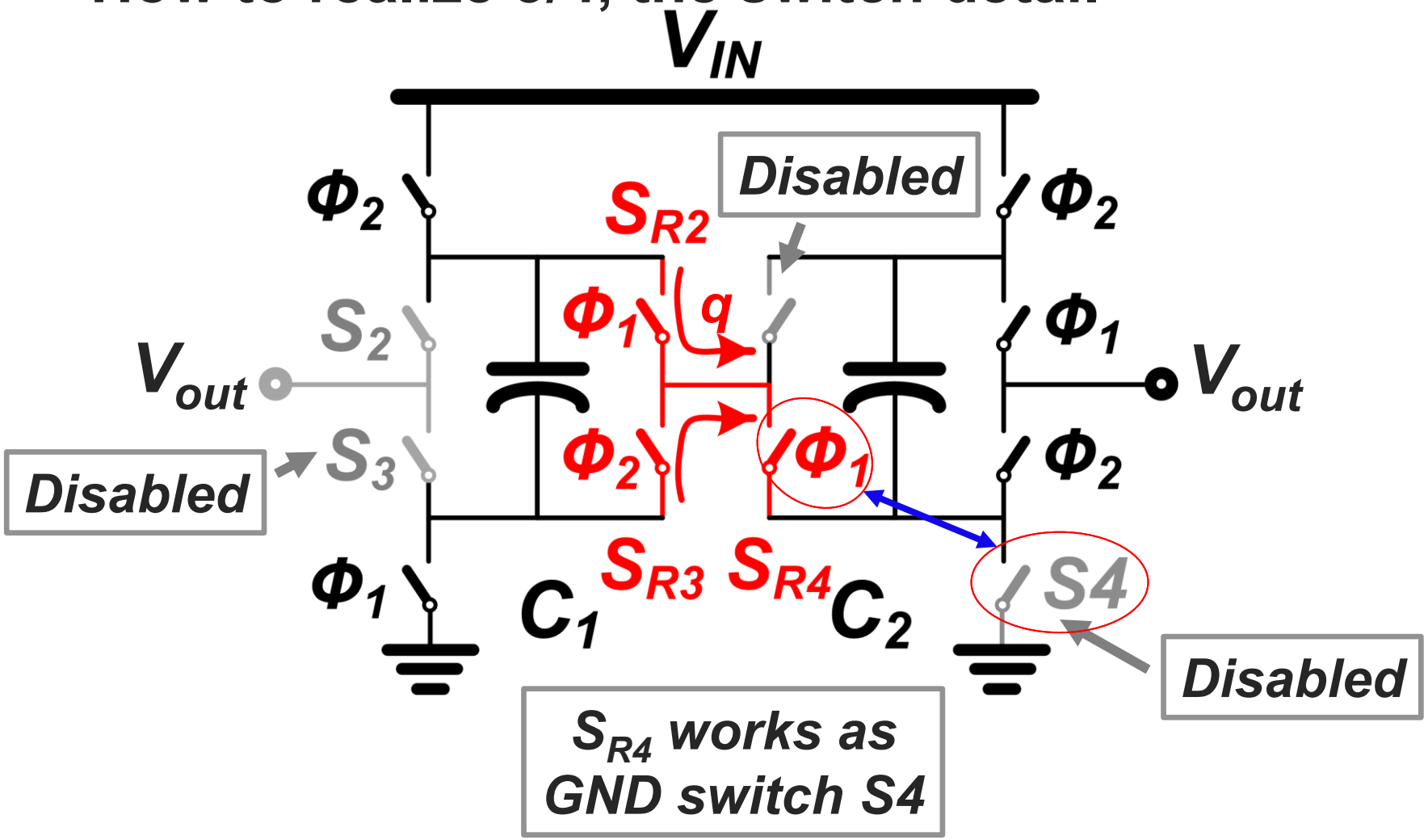


Ratio = 1/4
two cells in cascade

Recursive Inter-Cell Connection

- How to realize 3/4, the switch detail



Recursive Inter-Cell Connection

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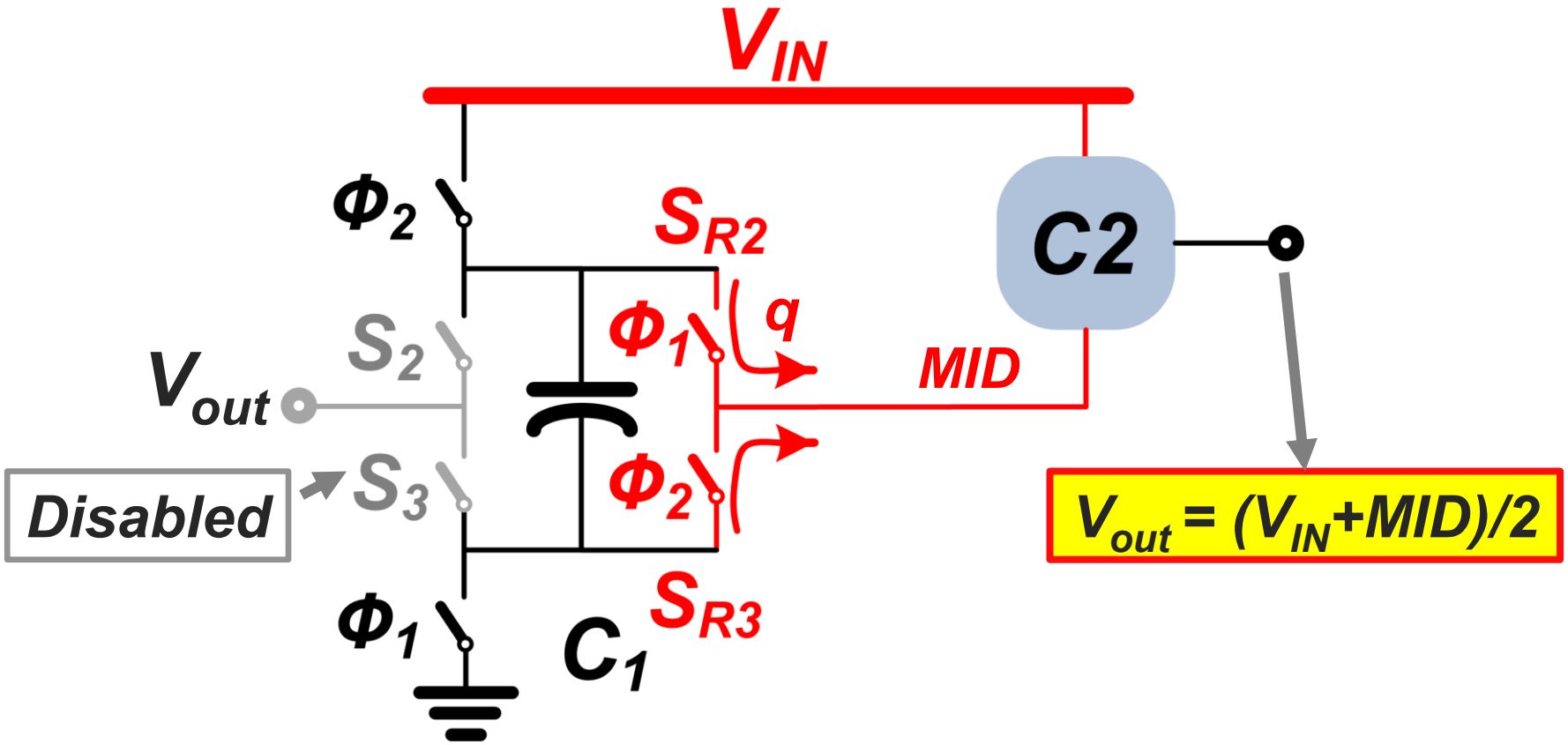
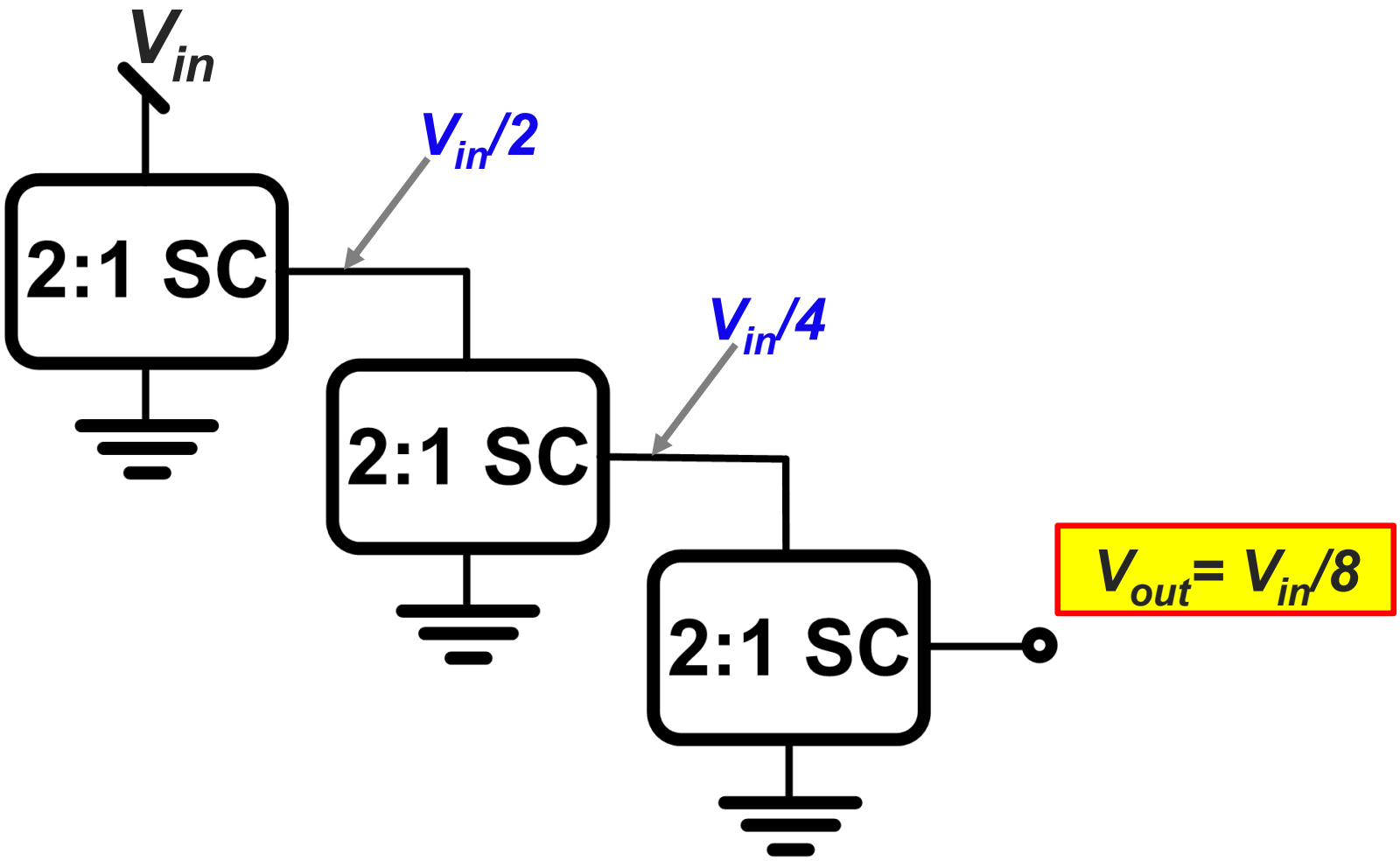


Ratio = 3/4
two cells are stacked

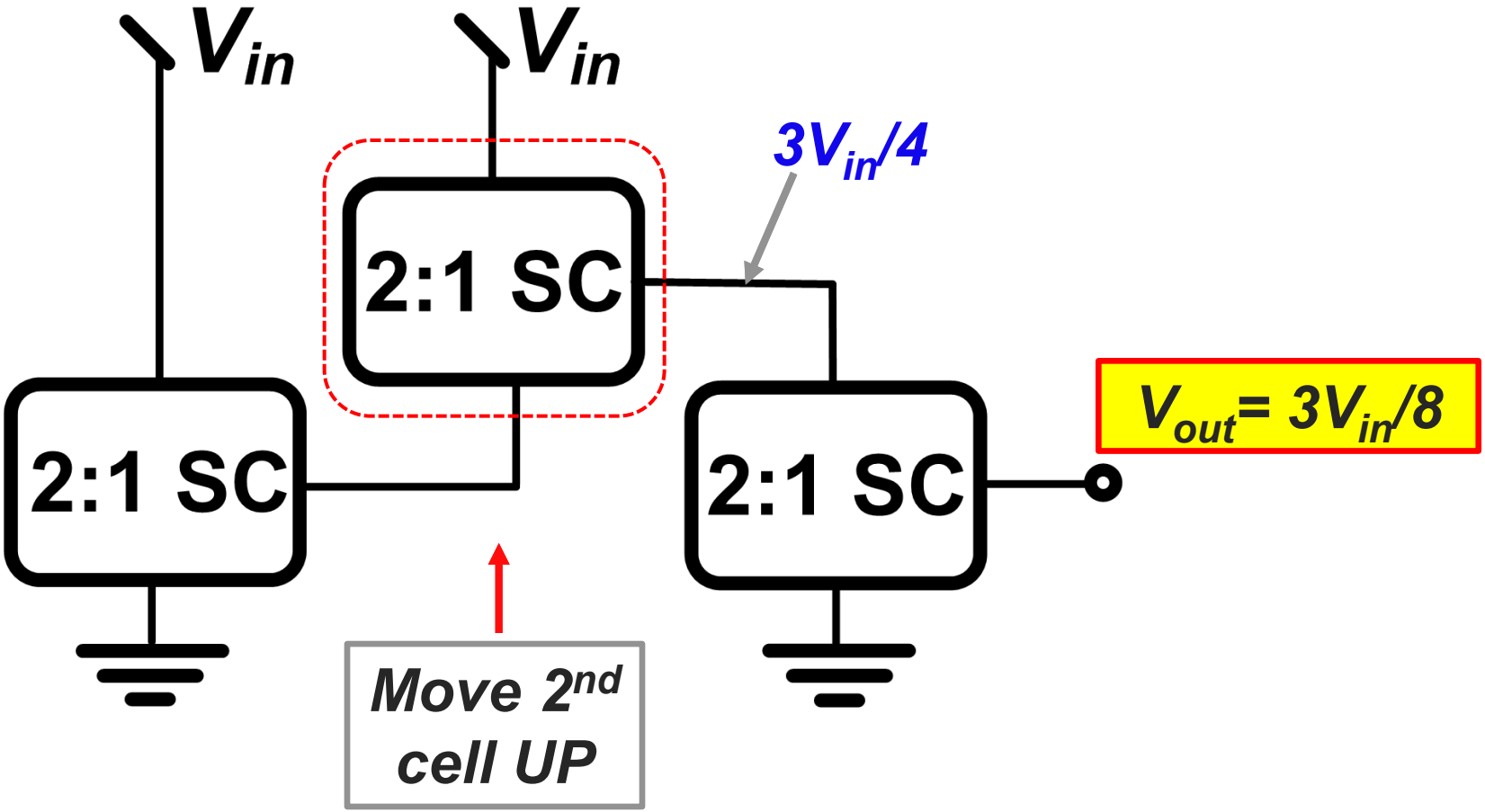
Recursive 3-bit SC

- Adding a third 2:1 SC cell: **resolution = $V_{in}/2^3$**



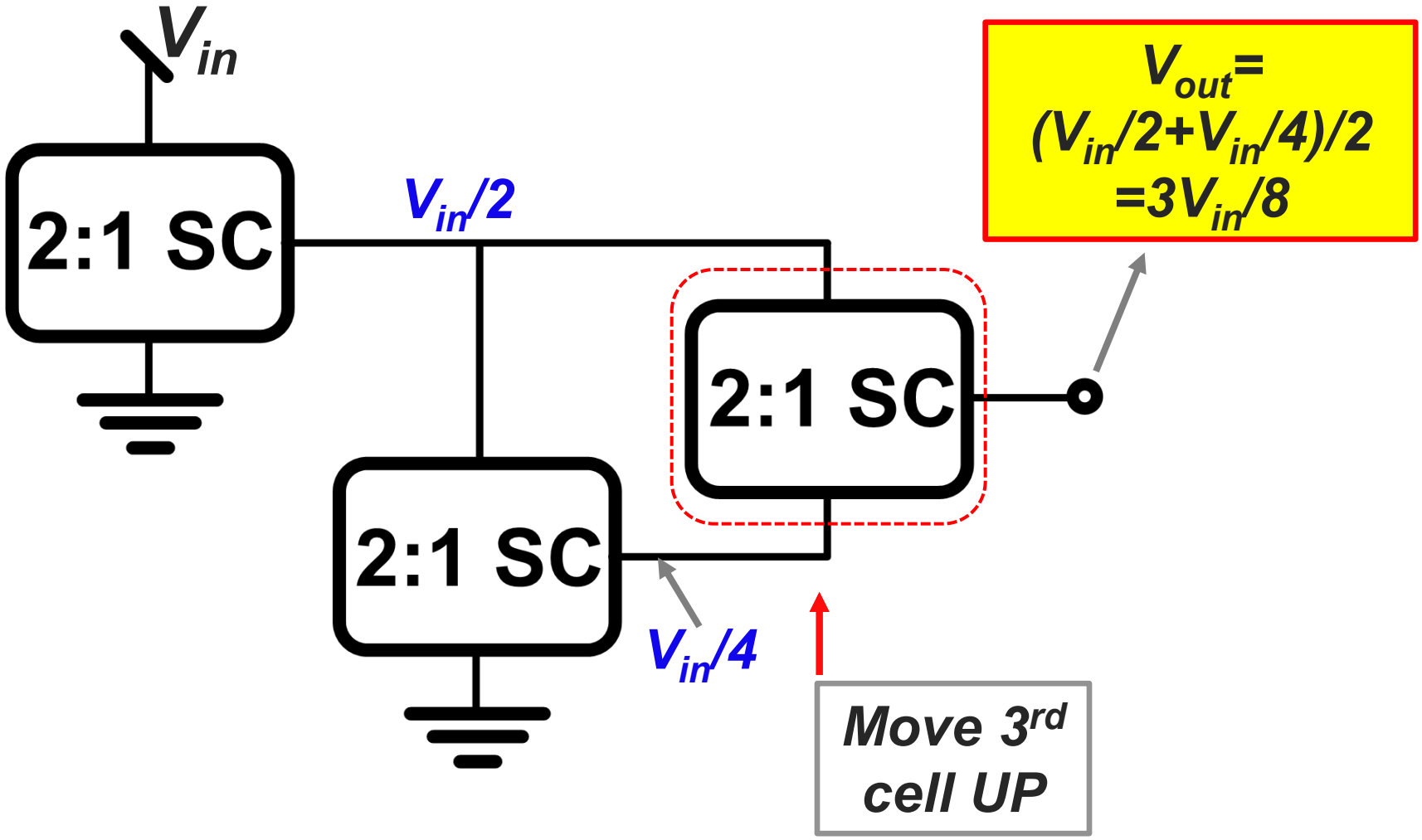
Recursive 3-bit SC

- **Realizing 3/8 ratio**



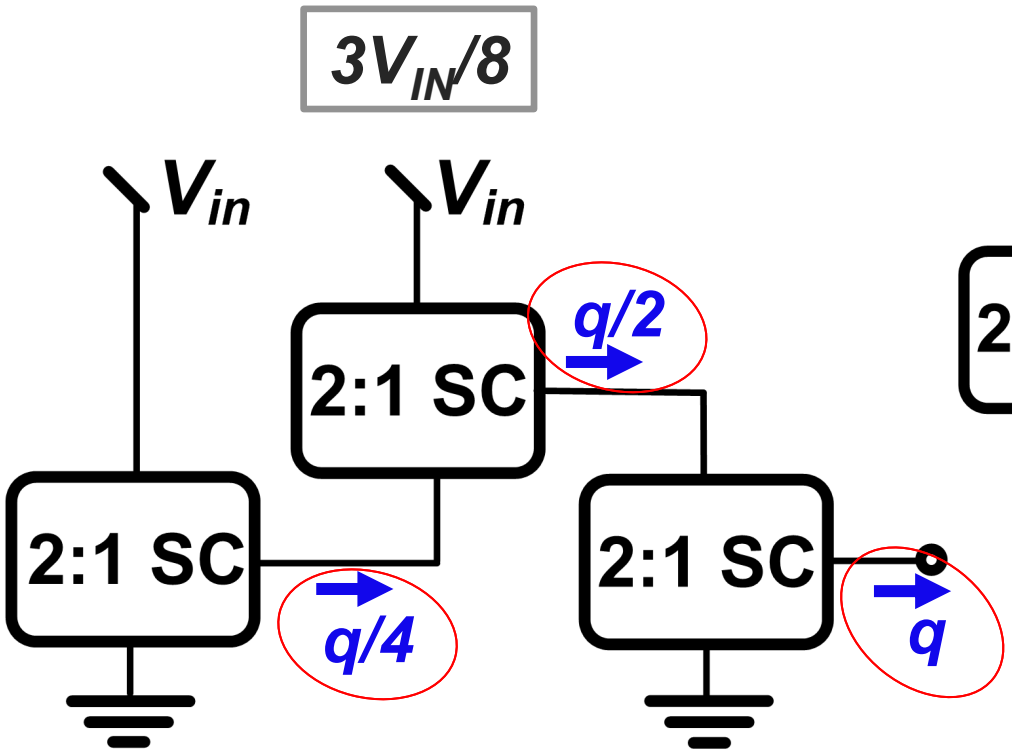
Recursive 3-bit SC

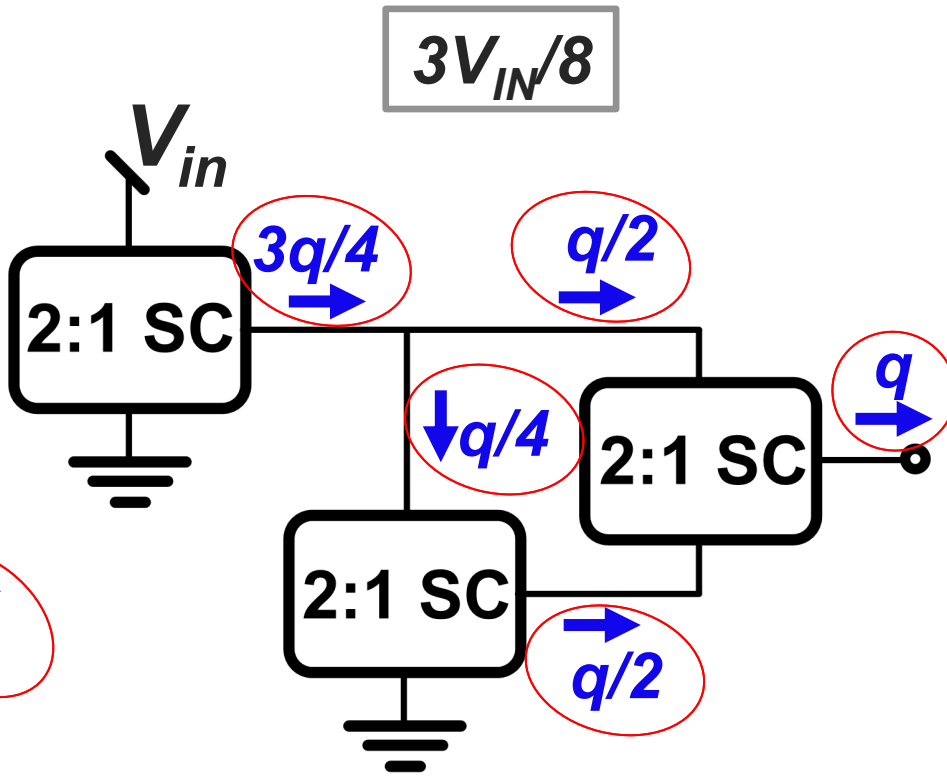
- Another way to realize 3/8 ratio



Recursive 3-bit SC

- Which one is better to realize 3/8 ratio?





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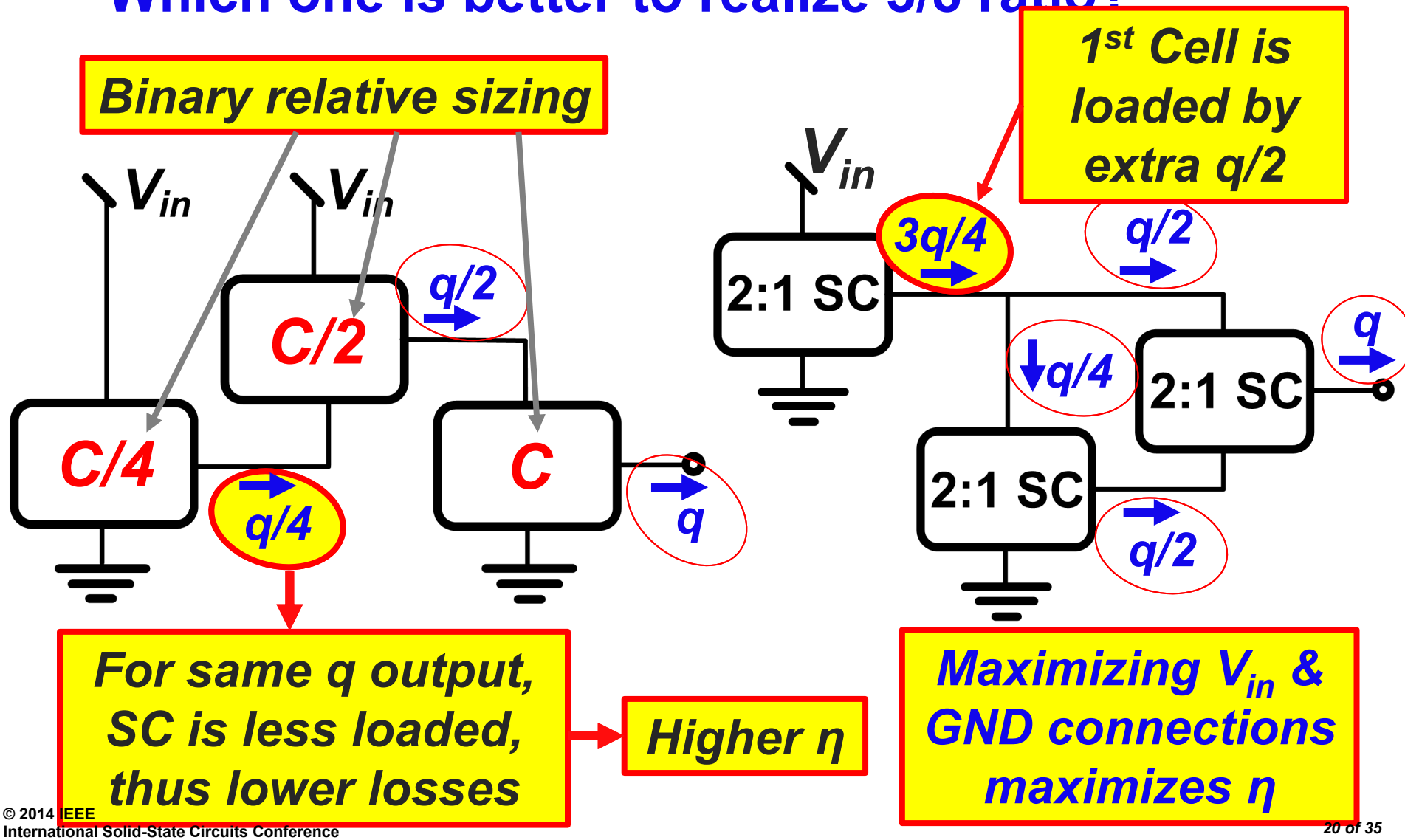
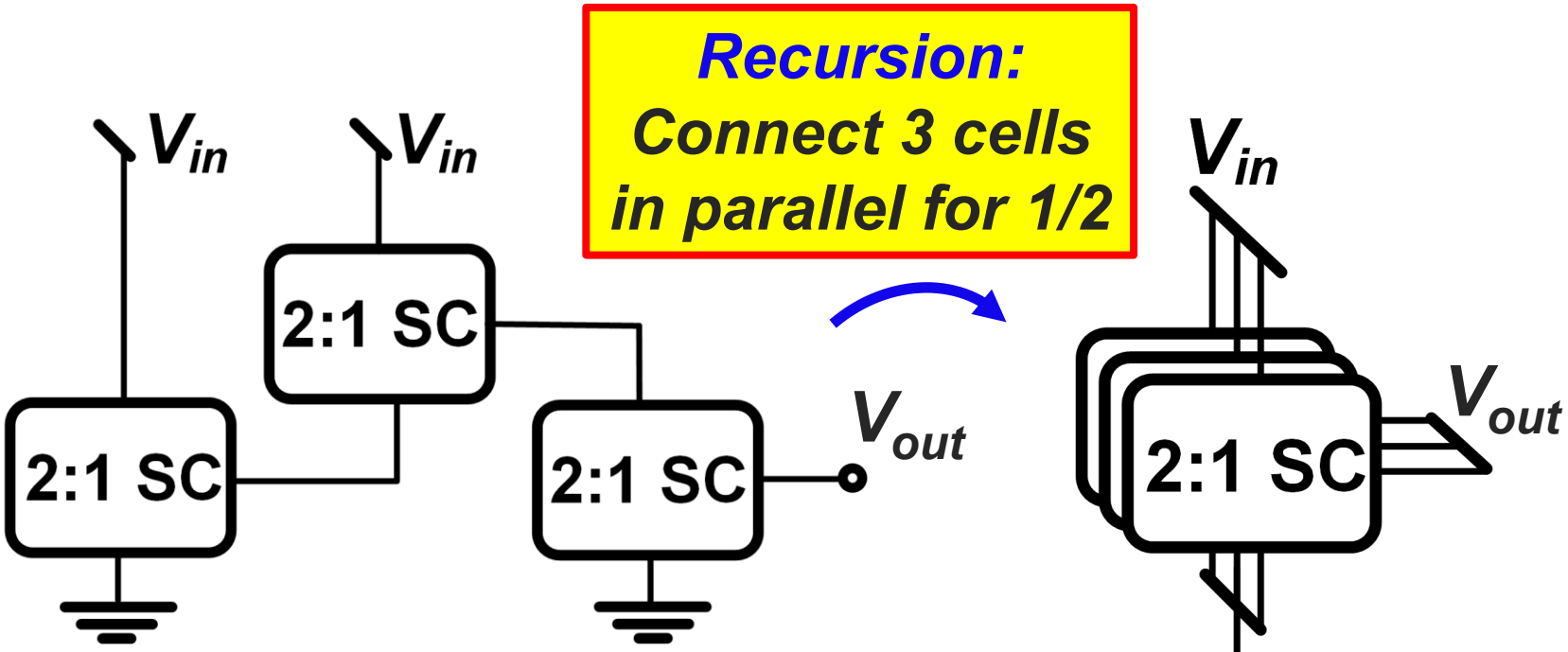


Recursive 3-bit SC: 1/2 Realization

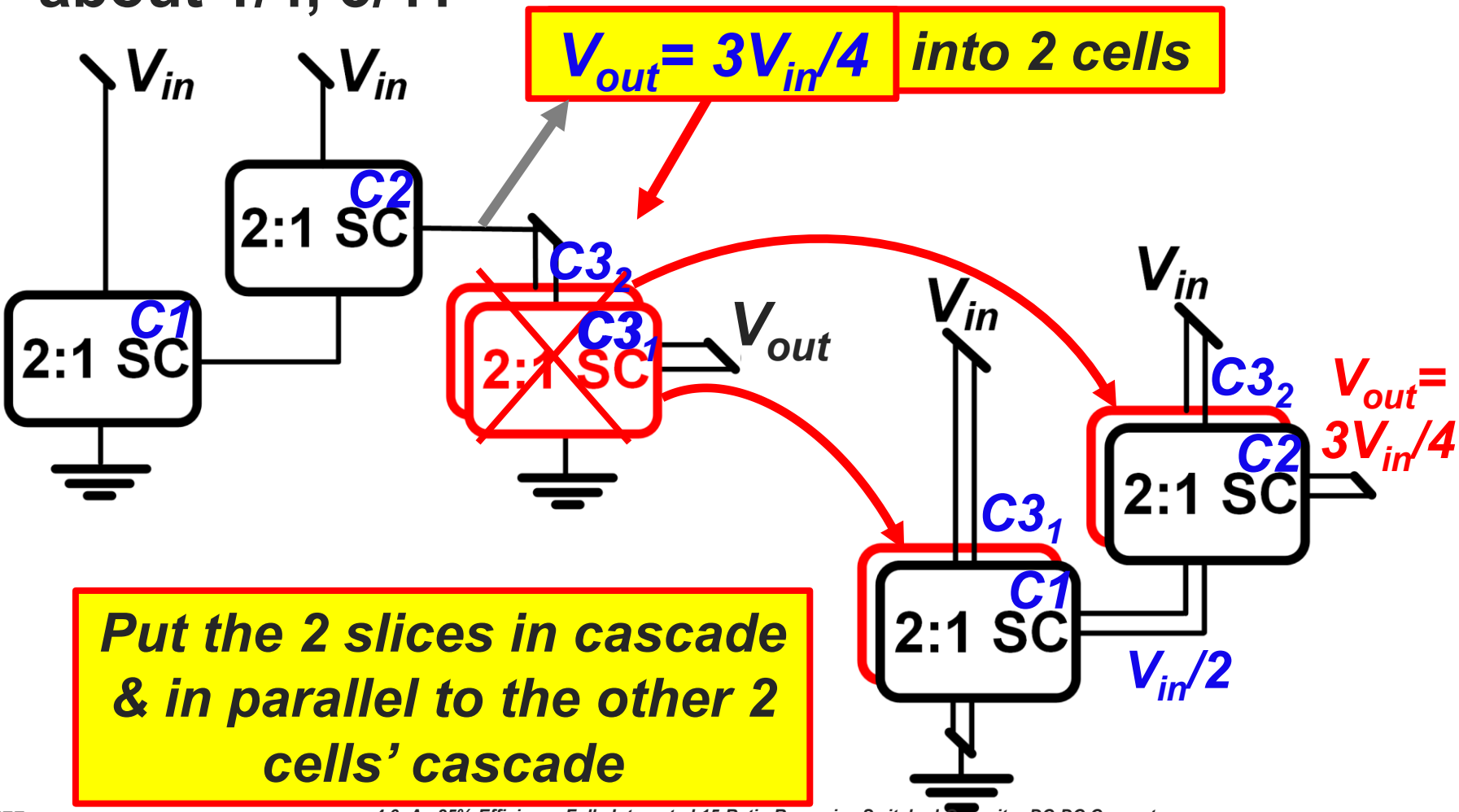
- Now 1/8, 3/8, 5/8, 7/8 are realized, how to achieve 1/2 using 3 cells?



Cells connected in cascade for $n_{odd}/8$

Recursive 3-bit SC: 1/4, 3/4 Realization

- Now 1/8, 3/8, 5/8, 7/8, and 1/2 are realized, what about 1/4, 3/4?



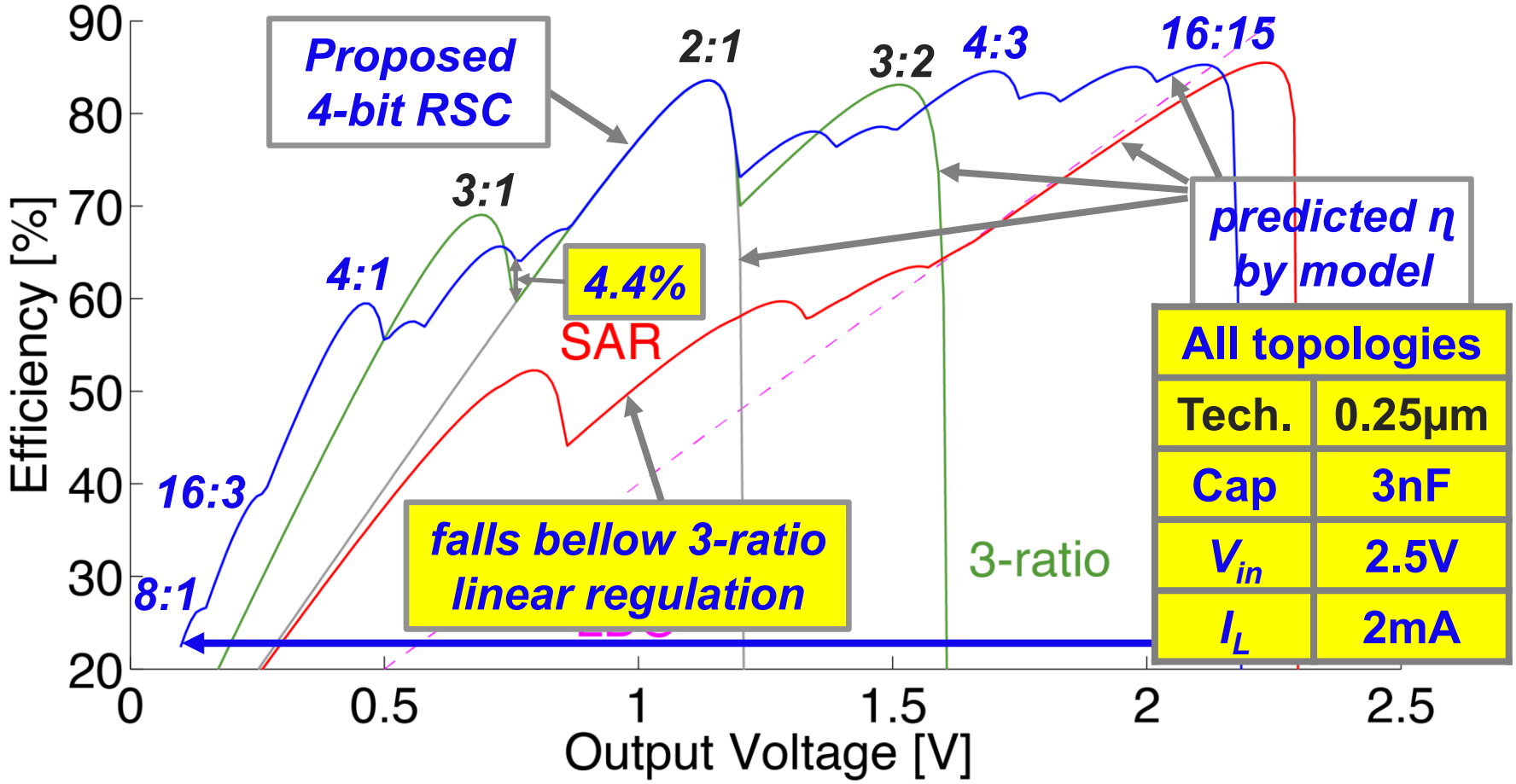
Recursive 4-bit SC

- A **4-bit Recursive SC** topology is implemented
  - *Balance between complexity and flat η*

Realizing 15-ratio, of high η by:

- ***Recursive inter-cell connection for 100% cap utilization***
- ***Maximizing V_{in} & GND connections***
- ***Binary relative sizing***

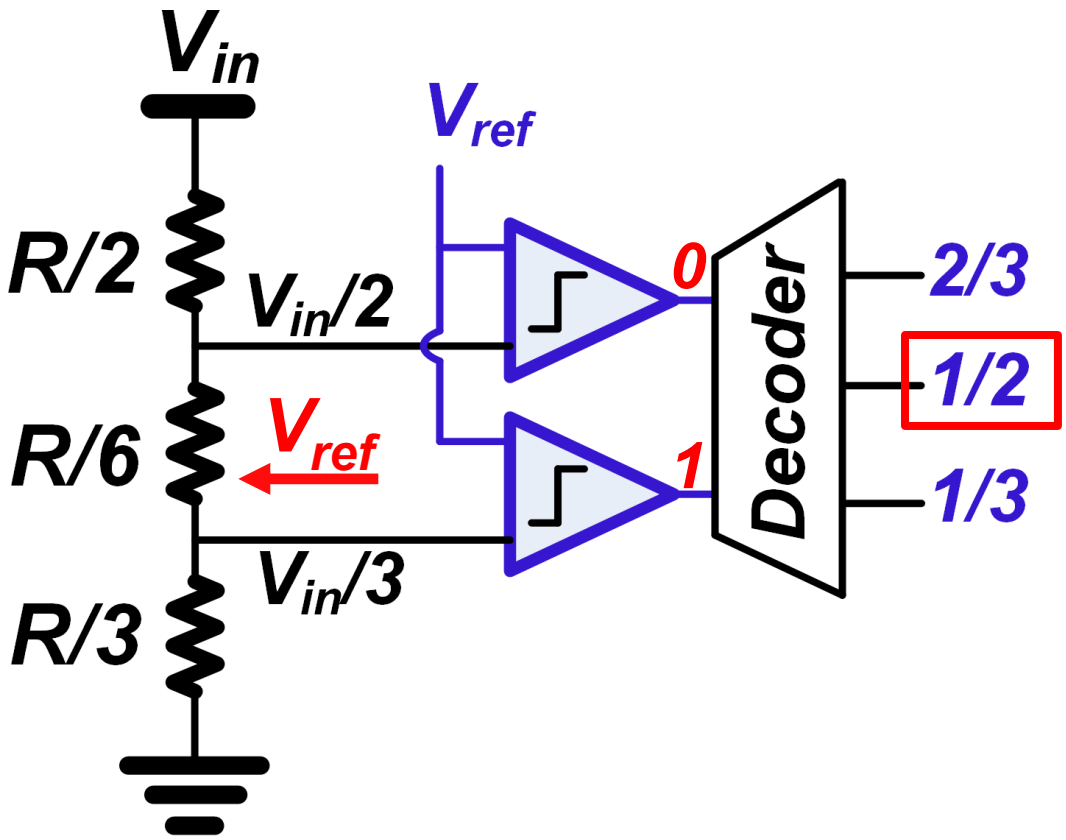
4-bit Recursive SC Efficiency vs. V_{out}



For same silicon area: widest operating range, highest average efficiency

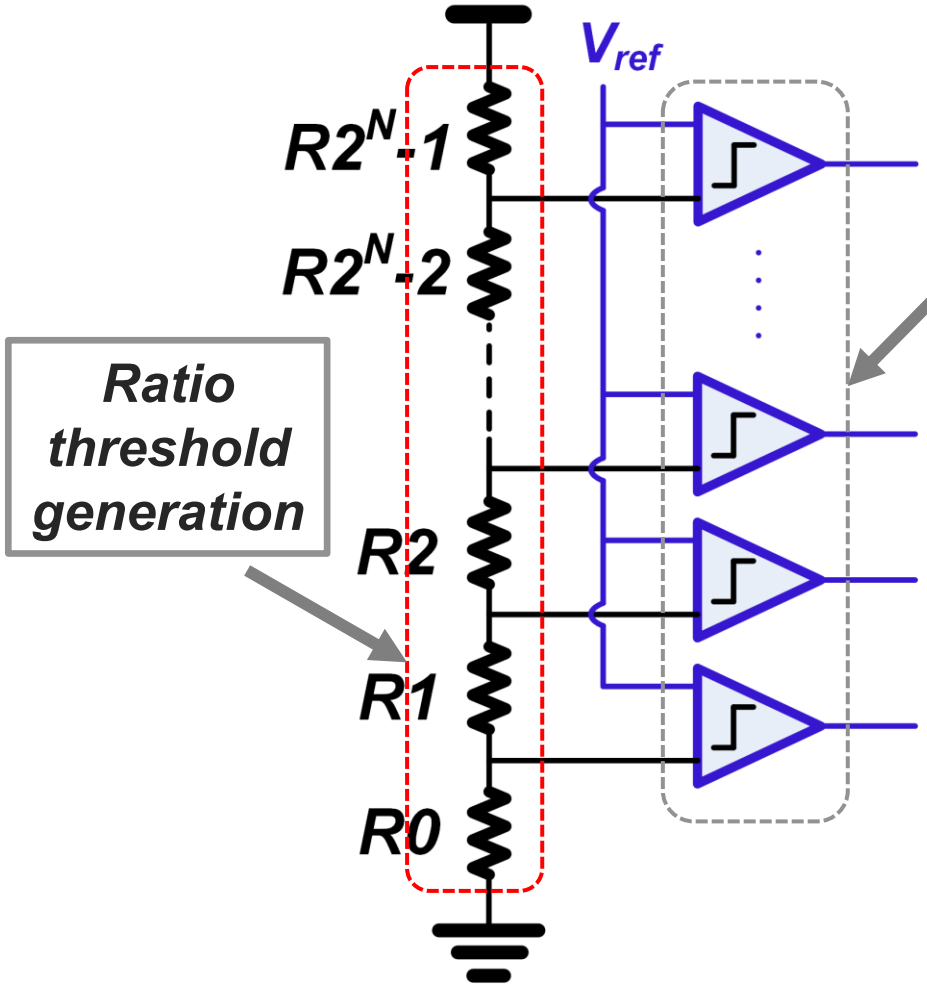
Typical Multi-Mode SC Control

- Compare V_{ref} (desired output) with levels from a resistor string to find desired ratio



Typical Multi-Mode SC Control

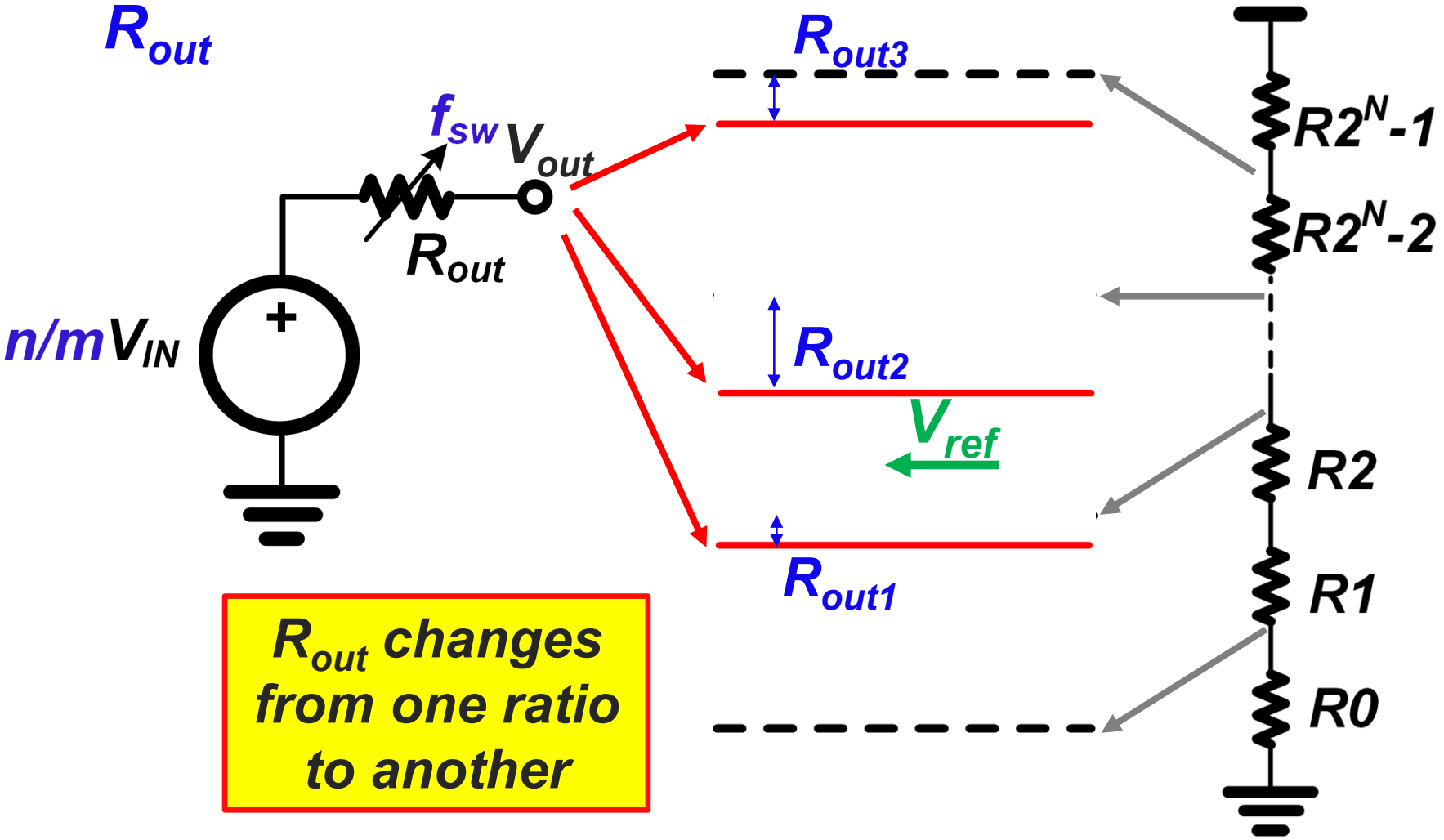
- Challenge of large number of ratios



For 8-bit resolution~256 accurate resistors and comparators are needed

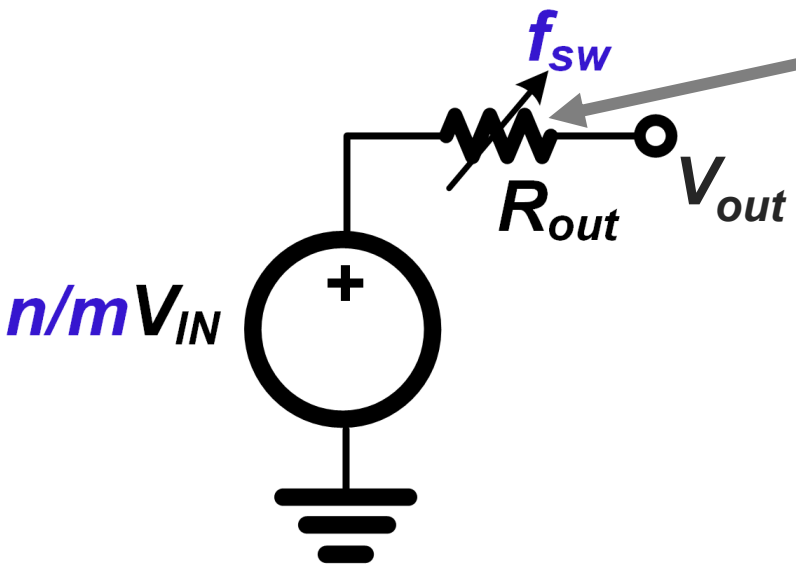
Typical Multi-Mode SC Control

- Ratios' threshold levels mismatch due to SC R_{out}



All-Digital Binary Search Control

- **Solution: Ratios' threshold levels are produced by the SC itself**

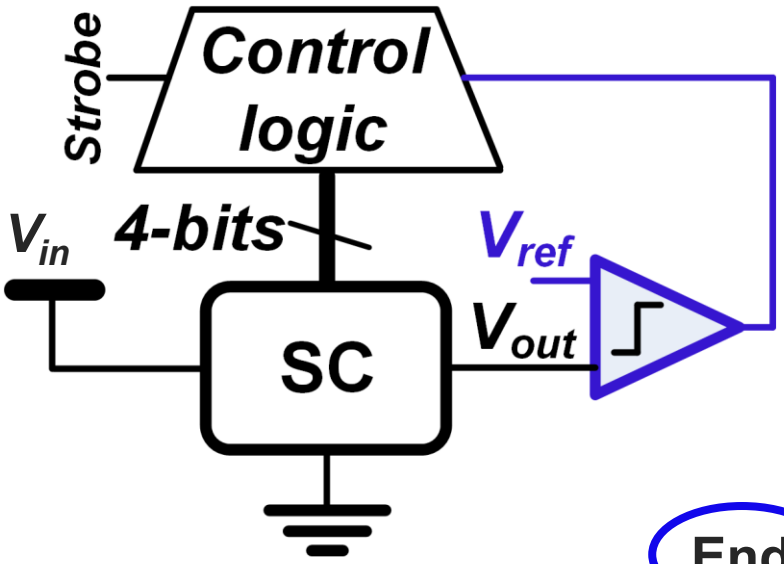


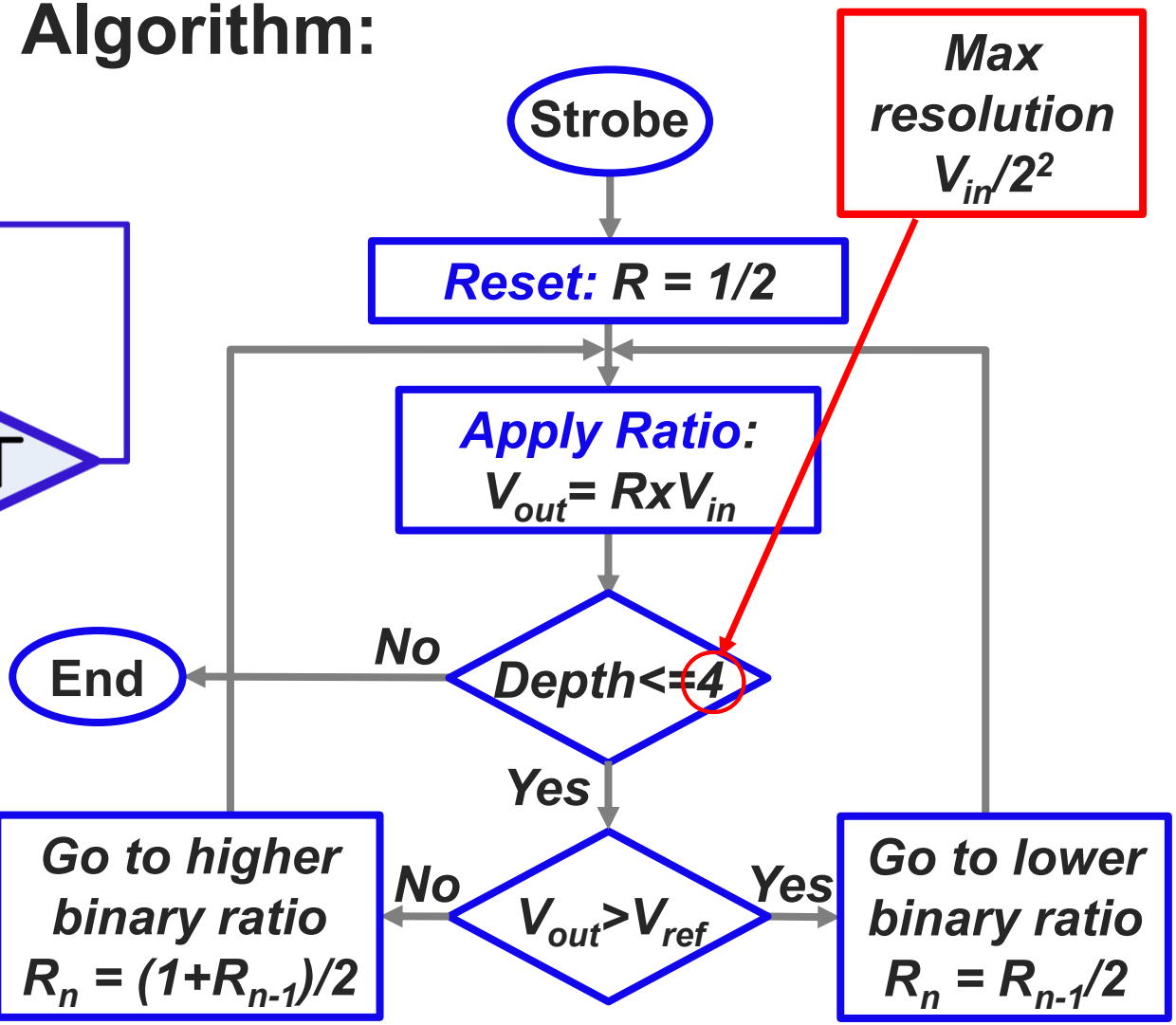
Switching at highest f_{sw}, R_{out} is min

SC outputs the max V_{out} for certain n/m RATIO

All-Digital Binary Search Control

- Binary Search Algorithm:

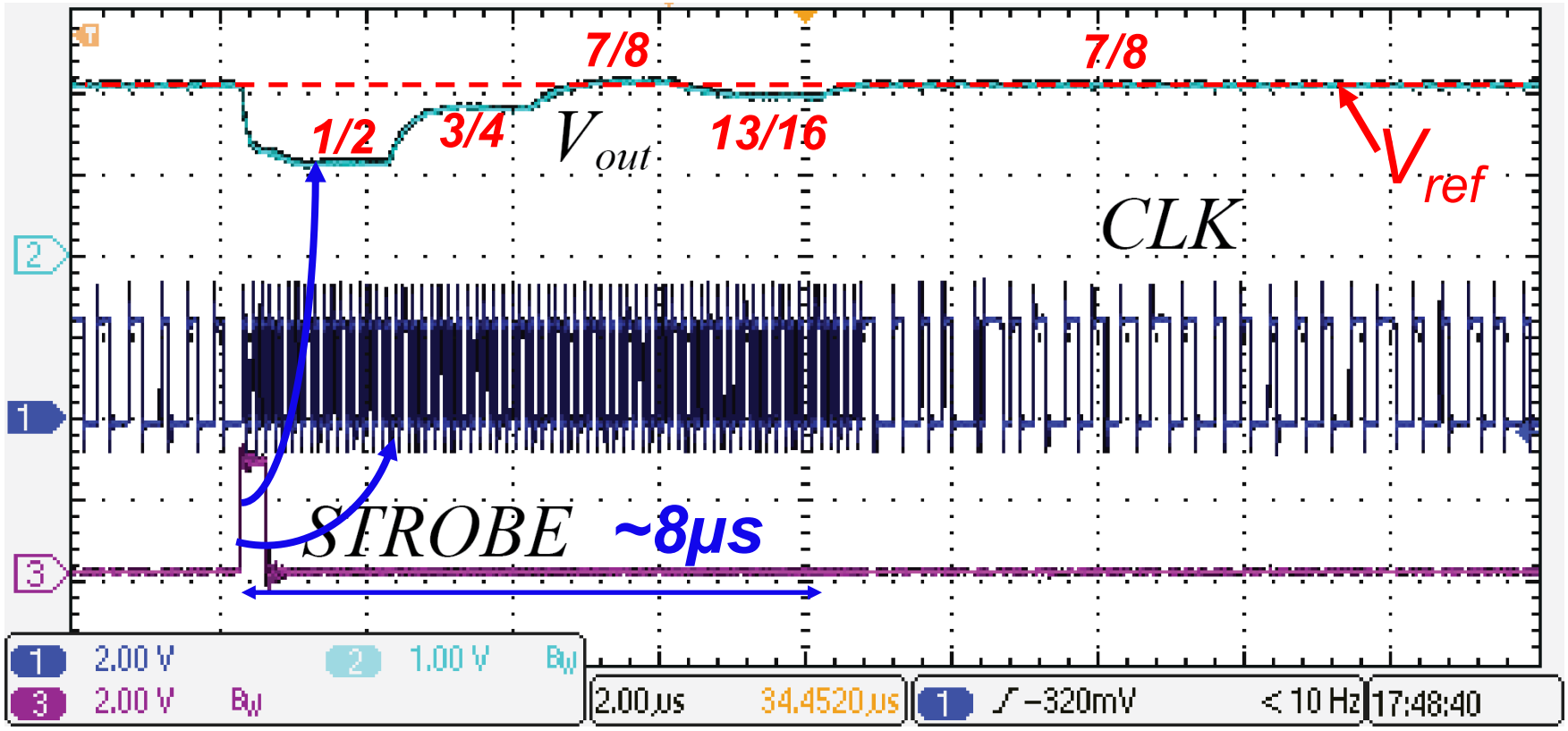




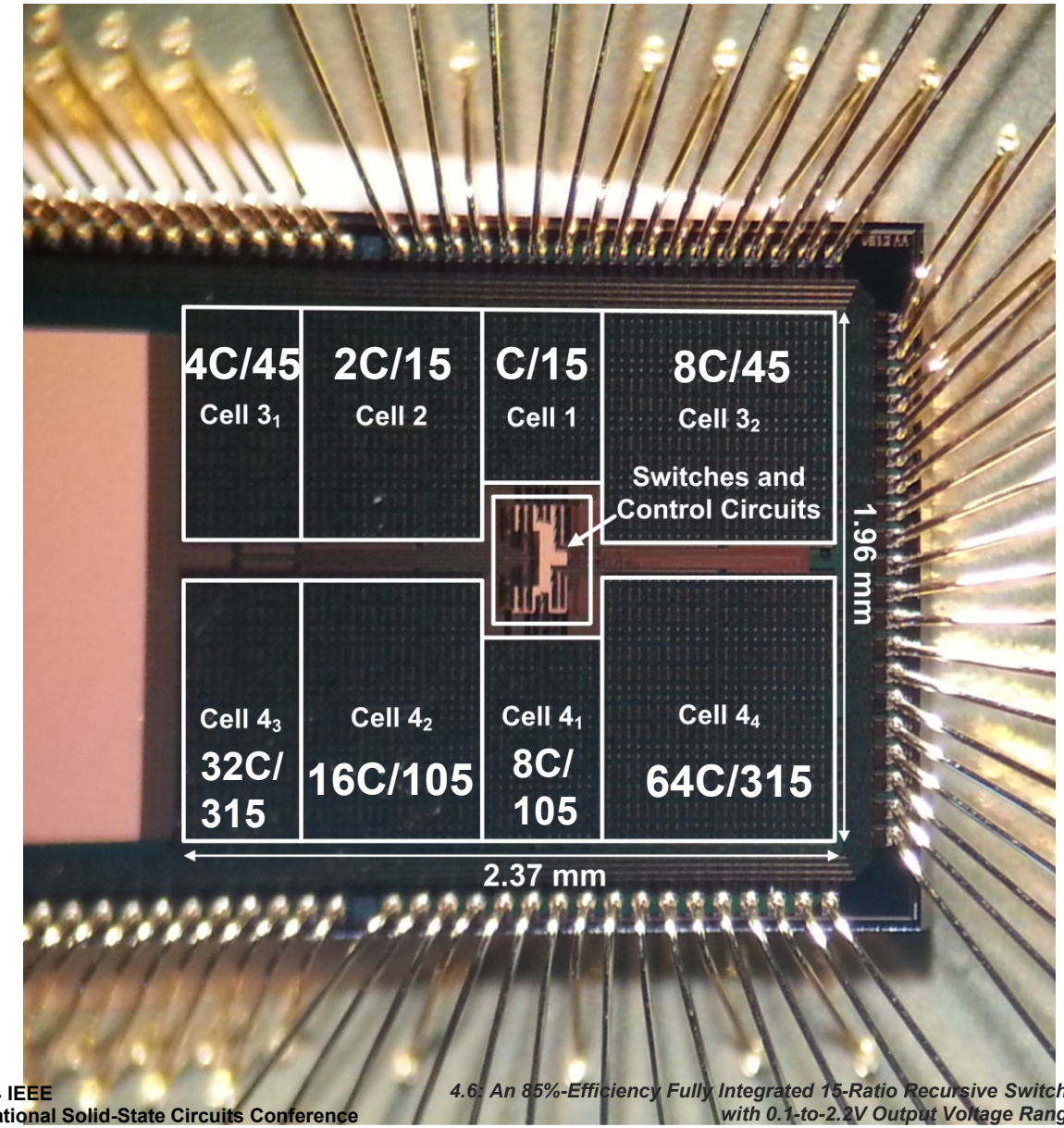
- *No resistor string*
- *1 comparator & simple gates*
- *No R_{out} mismatch*

Measured Controller Transient Response

- 8 µs response time



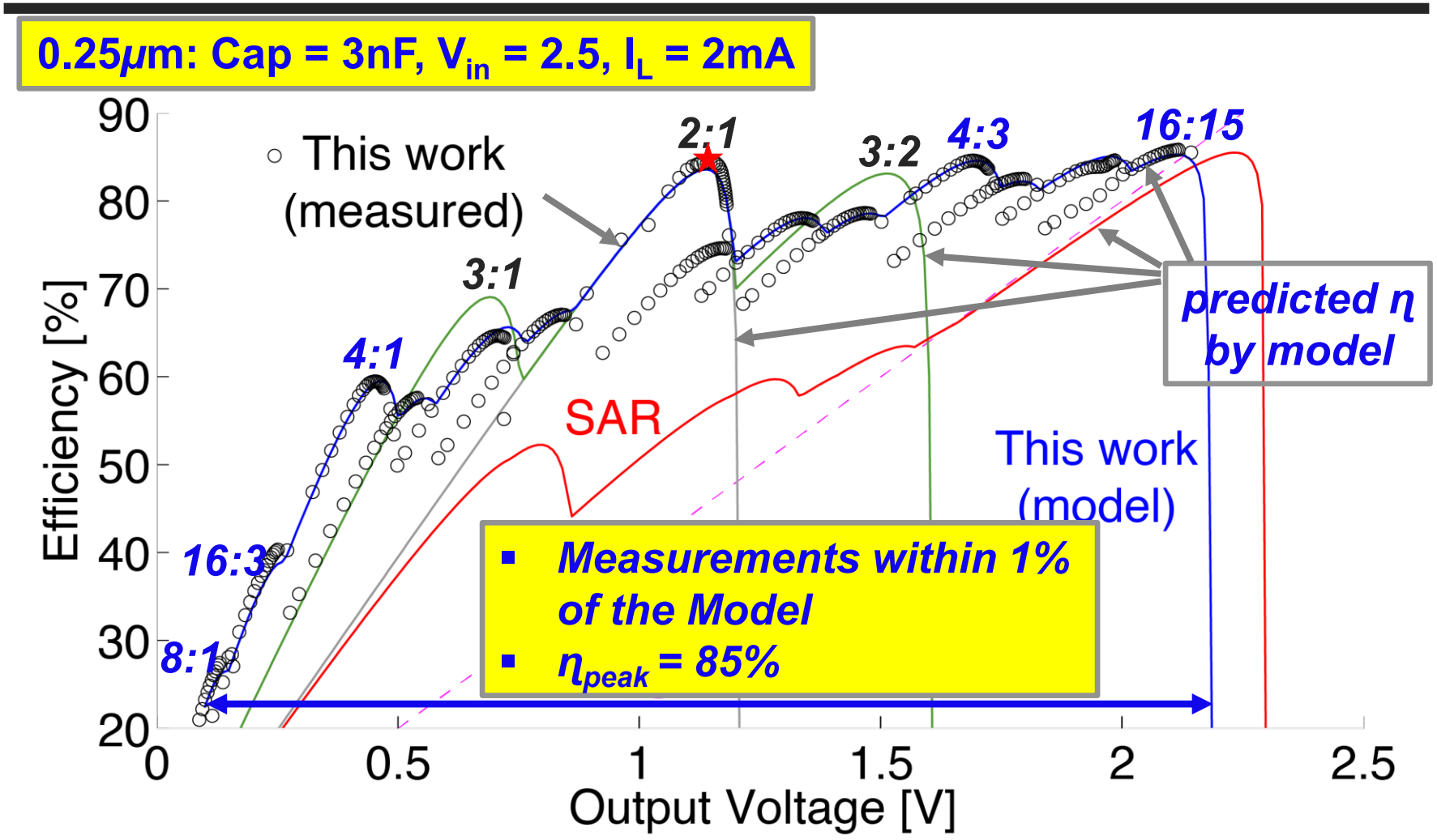
Fully Integrated Recursive 4-bit SC Prototype



0.25um 2.5V bulk CMOS MIM ~ 0.9 fF/um^2

- **8 2:1 cells are used to enable recursion**
- **Cells are binary weighted for optimal relative sizing**

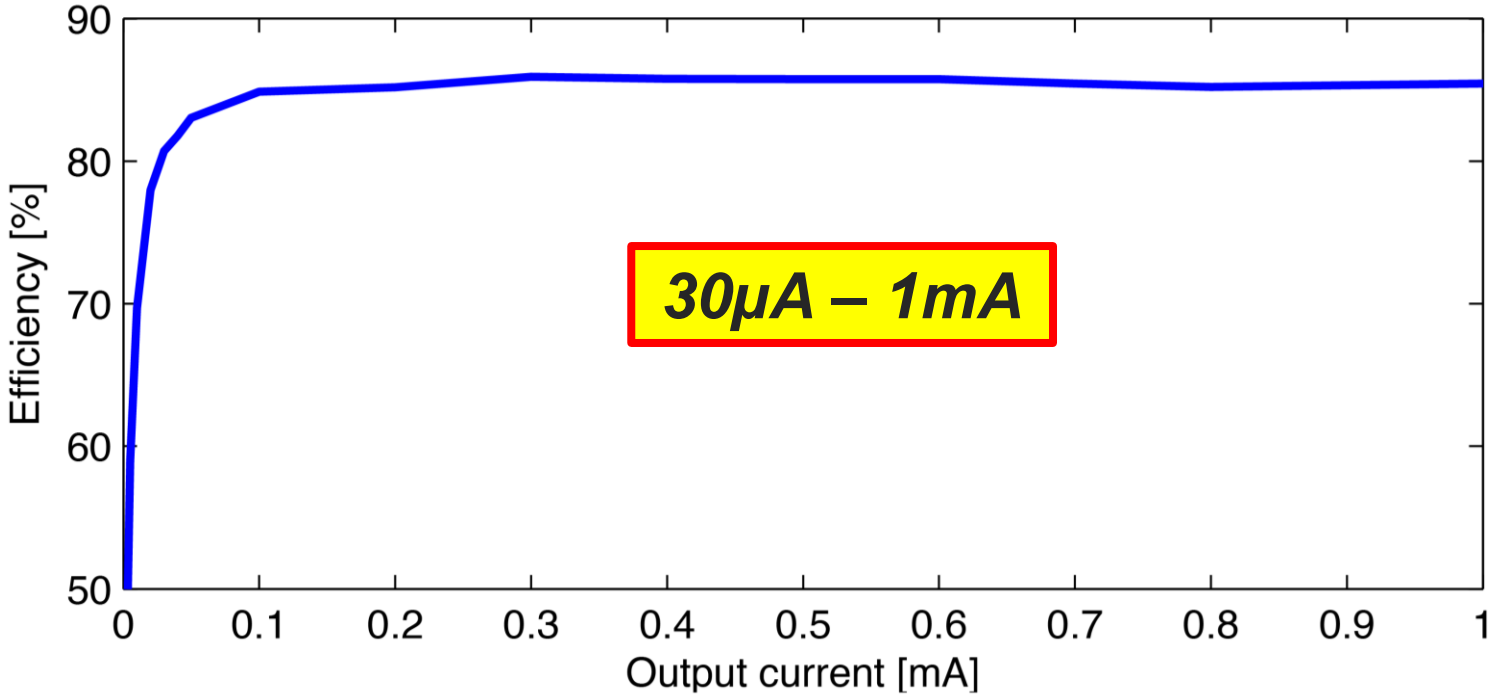
Measured Efficiency vs. V_{out}



For same silicon area: widest operating range, highest average efficiency

Measured Efficiency vs. I_L

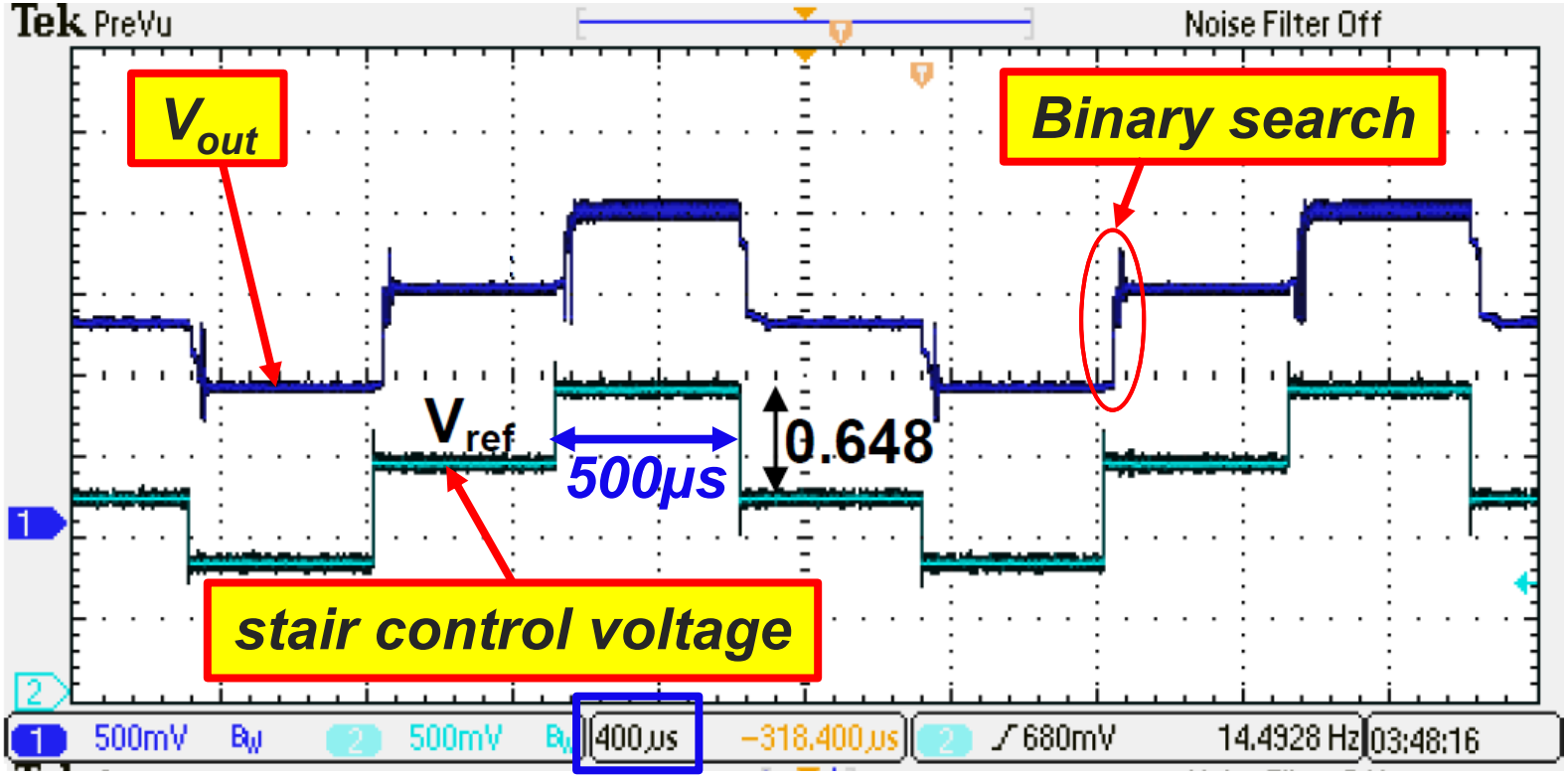
0.25μm: C = 3nF, V_{in} = 2.5, Ratio = 1/2



Switching losses scale with lower power levels

Measured Controller Transient Response

- Tracking an input stair control voltage



Conclusions

- **A new Modular SC topology comprising individual 2:1 SC**
- **High *η* through:**
  - ***Recursive interconnection* achieving 100% cap utilization**
  - ***Maximizing V_{in} & GND connections* for minimum overhead charge through the SC**
  - ***Optimal resource allocation* (*C*,*G*) through *BINARY* relative sizing**

Highest average η & widest operating range amongst other SC topologies for same silicon area